NXP Semiconductors
Product Brief

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Kinetis KL2x—Ultra-Low-Power MCUs with USB

Up to 512 KB of flash and 128 KB of SRAM

1. Kinetis L Family Introduction

The Kinetis L series MCUs combine the exceptional low-power performance, energy efficiency, and ease of use of the new ARM® Cortex®-M0+ processor with the performance, peripheral sets, enablement, and scalability of the Kinetis 32-bit MCU portfolio.
The Kinetis ultra-low-power L series frees the power-critical designs from 8- and 16-bit MCU limitations by combining excellent dynamic and stop currents with superior processing performance, a broad selection of on-chip flash memory densities, and extensive analog, connectivity, and HMI peripheral options.
Kinetis ultra-low-power L series MCUs are hardware- and software-compatible with the ARM-Cortex-M4-based Kinetis K series, providing a scalable migration path to higher performance, memory, and feature integration.

Contents

2. Kinetis KL2x Subfamily Overview

The Kinetis KL2x ultra-low-power MCU family features a full-speed USB 2.0 On-the-Go (OTG) controller or a full-speed crystal-less USB 2.0 device controller in addition to the Kinetis KL1x series. The Kinetis KL2x MCU family is also compatible with the Kinetis K20 MCU family (based on the ARM Cortex-M4 core), and with all other Kinetis KL1x, KL3x, and KL4x series MCUs, providing a migration path for lower and higher performance and feature integration.

- KL24—a broad offering with mixed signal integration and full-speed USB OTG 2.0.
- KL25—an expansion from the KL24 family with the addition of 16-bit ADC and TSI.
- KL26—an expansion from the KL25 family with up to 256 KB flash and 32 KB SRAM, together with the addition of I^2S and 16-bit SPI.
- KL27—up to 1:4 SRAM-to-flash ratio, device-only crystal-less USB 2.0, built-in ROM bootloader, enhanced mixed signal integration with high-accuracy VREF, ISO7816, two LPUARTs, FlexIO, and high-accuracy 48 MHz IRC.
- KL28—up to 512 KB flash, 128 KB SRAM, 72 MHz core frequency (up to 96 MHz for a high-speed run), advanced smart peripherals including LPUART, LPSPI, LPI2C, EVSIM, parallel FlexIO, crystal-less USB OTG, and others.

3. Kinetis KL2x Key Features

- Ultra-low-power 72 MHz MCUs supported with baseline functions, and with up to 512 KB flash and 128 KB RAM.
- Full-speed USB 2.0 OTG, or full-speed crystal-less USB 2.0 device controller supporting asynchronous wakeup on resume, signaling down to the STOP/VLPS modes.
- Asynchronous DMA enables energy-saving peripherals (for example, ADC, UART, and Timer/PWM) to trigger an asynchronous DMA request in the STOP/VLPS modes, to perform the DMA transfer and return to the current power mode without CPU intervention.
- LPUART supports asynchronous transmit and receive operations to the bus clock, supporting communication down to the STOP/VLPS modes. The configurable receiver baud-rate oversampling ratio from 4× to 32× enables higher baud rates with lower clock sources.
- SPI supports the slave mode address match wakeup function and the first message capture down to the STOP/VLPS modes.
- I^2C supports multiple address match wakeup functions down to the STOP/VLPS modes.
- FlexIO can emulate multiple serial interfaces (for example, UART, SPI, I^2C, IrDA), and is fully functional in the STOP/VLPS modes.
- LPTPM supports 16-bit timer input capture, output compare, and PWM functions, down to the STOP/VLPS modes.
- LPTMR supports 16-bit timer and pulse-counter functions in all power modes.
- RTC supports a 32-bit second counter with a second interrupt and a programmable alarm in all power modes, including the temperature and voltage compensation.

- ADC supports single conversions in multiple result registers down to the STOP/VLPS modes along with hardware averaging and automatic compare modes.
- CMP supports threshold-crossing detection in all power modes (except for VLLS0) along with a triggered compare mode for lower average power compares.
- DAC and VREF support static reference in all power modes (except for VLLS0).
- TSI supports wake-on capacitive touch on a single channel in all power modes.
- LLWU supports eight wakeup pins, the RESET and NMI wakeup pins, and energy-saving peripherals in the LLS and VLLSx modes.
- Outstanding low-power operation with the core mark currents down to 100 µA/MHz, the state retention stop mode down to 1.7 µA with 7.5 µS wake-up time, and the lowest power mode down to 87 nA.
- Highly reliable, fast-access flash memory with four levels of protection for code security/protection.
- Lower time to market with comprehensive enablement solutions, including SDK (drivers, libraries, stacks), IDE, bootloader, RTOS, online community, and more.

4. Kinetis KL2x Family Feature Summary

Table 1. Family feature summary

Subfamily	KL24	KL25	KL26	KL27	KL28
CPU frequency	48 MHz	48 MHz	48 MHz	48 MHz	72 MHz (up to 96 MHz)
Flash memory	32–64 KB	32–128 KB	32–256 KB	32–256 KB	256–512 KB
SRAM	4–8 KB	4–16 KB	4–32 KB	8–32 KB	128 KB
ROM bootloader	—	—	—	16 KB	32 KB
Analog	12-bit ADC, CMP	16-bit ADC, 12-bit DAC, CMP	16-bit ADC, 12-bit DAC, CMP	16-bit ADC, 12-bit DAC, CMP, VREF	16-bit ADC, 12-bit DAC, CMP, VREF
Full-speed USB (2.0 OTG)	Yes	Yes	Yes	Crystal-less USB	Crystal-less USB
Connectivity	UART, LPUART, SPI, I^2C	UART, LPUART, SPI, I^2C	UART, LPUART, SPI, I^2C, I^2S	UART w/ ISO7816, LPUART, SPI, I^2C, I^2S, FlexIO	EMVSIM, LPUART, LPSPI, LPI^2C, I^2S, FlexIO, TSI
Package options	32QFN, 48QFN, 64LQFP, 80LQFP	32QFN, 48QFN, 64LQFP, 80LQFP	32QFN, 48QFN, 64LQFP, 64MAPBGA, 100LQFP, 121MAPBGA, 36WLCSP	32QFN, 48QFN, 36XFBGA, 64LQFP, 64MAPBGA	100 LQFP

5. Kinetis KL2x Family Block Diagram

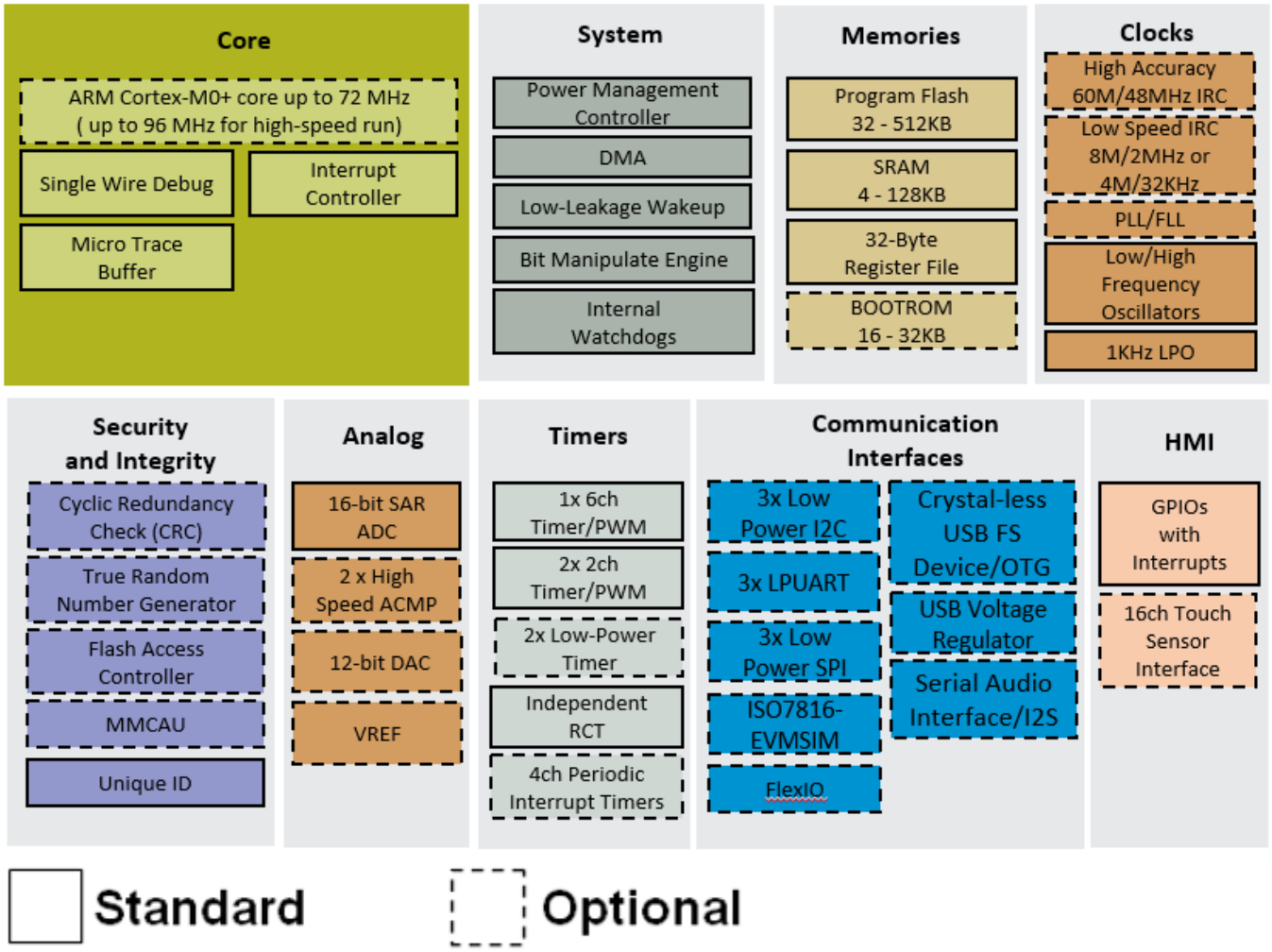

Figure 1. Kinetis KL2x family block diagram

6. KL2x Family Common Features

The following features are present on all KL2x MCUs:

- ARM Cortex-M0+ core running at up to 72 MHz (up to 96 MHz for high-speed run).
- 2-pin Serial Wire Debug (SWD), Micro Trace Buffer (MTB).
- 4–8-channel DMA controller.
- Integrated Bit Manipulation Engine (BME).
- 64 B cache and 32 B register file.
- 1 × 6-channel and 2 × 2-channel LPTPM.
- Low- and high-frequency OSC.
- RTC (32 KHz OSC).

- 1 × low-power timer, 1 × 2-channel PIT.
- Power Management Controller (PMC) with nine power modes.
- Non-Maskable Interrupt (NMI).
- Software and COP watchdog.
- Voltage range of 1.71–3.6 V.
- Temperature range (T_A) of -40–105 ºC.

7. Kinetis KL2x Family Differences

Table 2. Family differences

Subfamily		KL24	KL25	KL26	KL27	KL28
CPU frequency		48 MHz	48 MHz	48 MHz	48 MHz	72 MHz (up to 96 MHz)
Memory	Flash/SRAM size	32 KB/4–128 KB /16 KB	32 KB/4–128 KB /16 KB	32 KB/4–256 KB /32 KB	32 KB/8–128 KB /32 KB, 256 KB/32 KB	512 KB/128 KB
	ROM	—	—	—	16 KB	32 KB
Connectivity	USB	USB OTG 2.0 LS/FS	USB OTG 2.0 LS/FS	USB OTG 2.0 LS/FS	FS USB 2.0 Slave, Crystal-less USB	Crystal-less USB
	UART (LPUART /with ISO7816)	2(1 / –)	2(1 / –)	2(1 / –)	2(2 / 1)	3(3 / –)
	SPI	2[1]	2[1]	2[2]	2[2]	3[6]
	I^2C	2	2	2	2[3]	3[6]
	I^2S	—	—	1	1	1
	FlexIO	—	—	—	YES	YES[7]
	EMVSIM	—	—	—	—	1
Analog modules	ADC	12-bit	16-bit	16-bit	16-bit	16-bit
	ADC channels (SE/DE)	7/0–16/0	7/0–16/2	7/0–20/4	7/0–17/2	—
	DAC	—	12-bit	12-bit	Optional[4]	12-bit
	VREF	—	—	—	YES	YES
Other modules	CRC	—	—	—	Optional[5]	YES
	Security	—	—	—	—	MMCAU, FAC, TRNG
	TSI	—	9 ch–16 ch	9 ch–16 ch	—	16 ch
	Total GPIOs	23–66	23–66	23–80	23–51	82
	MCG	4 MHz/32 KHz IRC PLL/FLL	4 MHz/32 KHz IRC PLL/FLL	4 MHz/32 KHz IRC PLL/FLL	High-accuracy 48 MHz IRC, 8/2 MHz IRC	High-accuracy 60/48 MHz IRC, 8/2 MHz IRC,

Table 2. Family differences

Subfamily	KL24	KL25	KL26	KL27	KL28
					PLL
Package options	32QFN, 48QFN, 64LQFP, 80LQFP	32QFN, 48QFN, 64LQFP, 80LQFP	32QFN,48QFN, 64LQFP, 64MAPBGA, 100LQFP, 121MAPBGA 36WLCSP	32QFN, 48QFN, 64LQFP, 64MAPBGA, 36XFBGA	100LQFP

[1]8-bit SPI, one SPI with FiFo
[2]16-bit SPI, one SPI with FiFo
[3]Double buffering with support up to 1 Mbps
[4]DAC is only available in 128 KB and 256 KB Flash KL27
[5]CRC is only available in 32 KB and 64 KB Flash KL27
[6]LPSPI and LPI2C
[7]Support parallel mode

8. Comprehensive Enablement Solutions

8.1. Kinetis Software Development Kit (SDK)

- Extensive suite of robust peripheral drivers, stacks, and middleware.
- Includes software examples demonstrating the usage of HAL, peripheral drivers, middleware, and RTOSes.
- Operating System Abstraction (OSA) for Freescale MQX RTOS, FreeRTOS, and Micrium µC/OS® kernels and bare-metal (no RTOS) applications.

8.2. Processor Expert

- Free software generation tool for device drivers/start-up code.
- Seven steps from project creation to debug—dramatically reduces the development time.
- Available within Kinetis Design Studio or as a standalone plug-in for IAR®/Keil®/GNU IDEs.

8.3. Integrated Development Environments (IDEs)

- Atollic TrueSTUDIO® IDE www.atollic.com/index.php/partnerfreescale
- Green Hills Software MULTI® IDE www.ghs.com/products/kinetis.html
- IAR Embedded Workbench® IDE www.iar.com/kinetis
- ARM Keil® Microcontroller Development Kit IDE www.keil.com/freescale

- Kinetis Design Studio IDE.
  - No-cost IDE for Kinetis MCUs.
  - Eclipse and GCC-based IDE for C/C++ editing, compiling, and debugging.
- Broad ARM ecosystem support through Freescale Connect partners.

8.4. Online enablement with ARM mbed™ development platform

- Rapid and easy Kinetis MCU prototyping and development.
- Online mbed SDK, developer community.
- Free software libraries.

8.5. MQX Lite RTOS

- Free, light-weight MQX kernel customized for small-resource MCUs.
- Packaged as a Processor Expert component.
- Upwards compatible with MQX RTOS.

8.6. Bootloader

- Common bootloader for all Kinetis MCUs.
- In-system flash programming over a serial connection: erase, program, verify.
- ROM- or flash-based bootloader with open-source software and host-side programming utilities.

8.7. Development hardware

- Tower System modular development platform:
  - Modular and expandable.
  - Rapid prototyping and evaluation.
  - Cost-effective.
- Freedom development platform:
  - Designed in an industry-standard compact form factor.
  - Integrated open-standard serial and debug interface (OpenSDA).
  - Compatible with a rich set of third-party expansion boards.
  - Low cost (< $20)

9. Part Identification

9.1. Description

The chip part numbers have fields that identify the specific part. Use the values of these fields to determine the specific part you received.

9.2. Format

The part numbers for this device have this format: Q KL## A FFF T PP CC (N)

9.3. Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 3. Part number field descriptions

Field	Description	Values
Q	Qualification status	M = fully qualified, general market flow P = prequalification
KL##	Kinetis family	KL24 KL25 KL26 KL27 KL28
A	Key attribute	Z = Cortex-M0+
FFF	Program flash memory size	32 = 32 KB 64 = 64 KB 128 = 128 KB 256 = 256 KB 512 = 512 KB
R	Silicon revision	(Blank) = main A = revision after main
T	Temperature range	V = -40–105 °C
PP	Package identifier	FM = 32QFN (5 mm × 5 mm) AL = 36WLCSP (2.4 mm × 2.5 mm) DA = 36XFBGA (3.5 mm × 3.5 mm) FT = 48QFN (7 mm × 7 mm) LH = 64LQFP (10 mm × 10 mm) MP = 64MAPBGA (5 mm × 5 mm) LK = 80LQFP (12 mm × 12 mm) LL = 100LQFP (14 mm × 14 mm) MC = 121MAPBGA (8 mm × 8 mm) DC = 121XFBGA (8 mm × 8 mm)
CC	Maximum CPU frequency (MHz)	4 = 48 MHz 7 = 72 MHz

Table 3. Part number field descriptions

Field	Description	Values
N	Packaging type	R = tape and reel (Blank) = trays

10. Orderable Part Numbers

Table 4. Ordering information

Product	Memory		Package		IO and ADC channel		
MC part number	Flash	SRAM	Pin count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC channels (SE/DP)
MKL24Z32VFM4	32 KB	4 KB	32	QFN	23	19/4	7/0
MKL24Z32VFT4	32 KB	4 KB	48	QFN	36	24/4	14/0
MKL24Z32VLH4	32 KB	4 KB	64	LQFP	50	31/4	16/0
MKL24Z32VLK4	32 KB	4 KB	80	LQFP	66	39/4	16/0
MKL24Z64VFM4	64 KB	8 KB	32	QFN	23	19/4	7/0
MKL24Z64VFT4	64 KB	8 KB	48	QFN	36	24/4	14/0
MKL24Z64VLH4	64 KB	8 KB	64	LQFP	50	31/4	16/0
MKL24Z64VLK4	64 KB	8 KB	80	LQFP	66	39/4	16/0
MKL25Z128VFM4	128 KB	16 KB	32	QFN	23	12/2	7/0
MKL25Z128VFT4	128 KB	16 KB	48	QFN	36	16/4	14/1
MKL25Z128VLH4	128 KB	16 KB	64	LQFP	50	19/4	16/2
MKL25Z128VLK4	128 KB	16 KB	80	LQFP	66	23/4	16/2
MKL25Z32VFM4	32 KB	4 KB	32	QFN	23	12/2	7/0
MKL25Z32VFT4	32 KB	4 KB	48	QFN	36	16/4	14/1
MKL25Z32VLH4	32 KB	4 KB	64	LQFP	50	19/4	16/2
MKL25Z32VLK4	32 KB	4 KB	80	LQFP	66	23/4	16/2
MKL25Z64VFM4	64 KB	8 KB	32	QFN	23	12/2	7/0
MKL25Z64VFT4	64 KB	8 KB	48	QFN	36	16/4	14/1
MKL25Z64VLH4	64 KB	8 KB	64	LQFP	50	19/4	16/2
MKL25Z64VLK4	64 KB	8 KB	80	LQFP	66	23/4	16/2
MKL26Z128CAL4	128 KB	16 KB	36	WLCSP	23	12/2	7/0
MKL26Z128VFM4	128 KB	16 KB	32	QFN	23	19/4	7/0
MKL26Z128VFT4	128 KB	16 KB	48	QFN	36	24/4	14/1
MKL26Z128VLH4	128 KB	16 KB	64	LQFP	50	31/4	16/2
MKL26Z128VLL4	128 KB	16 KB	100	LQFP	80	42/4	20/4

Table 4. Ordering information

Product	Memory		Package		IO and ADC channel		
MC part number	Flash	SRAM	Pin count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC channels (SE/DP)
MKL26Z128VMC4	128 KB	16 KB	121	MAPBGA	80	42/4	20/4
MKL26Z128VMP4	128 KB	16 KB	64	MAPBGA	50	31/4	16/2
MKL26Z256VLH4	256 KB	32 KB	64	LQFP	50	31/4	16/2
MKL26Z256VLL4	256 KB	32 KB	100	LQFP	80	42/4	20/4
MKL26Z256VMC4	256 KB	32 KB	121	MAPBGA	80	42/4	20/4
MKL26Z256VMP4	256 KB	32 KB	64	MAPBGA	50	31/4	16/2
MKL26Z32VFM4	32 KB	4 KB	32	QFN	23	19/4	7/0
MKL26Z32VFT4	32 KB	4 KB	48	QFN	36	24/4	14/1
MKL26Z32VLH4	32 KB	4 KB	64	LQFP	50	31/4	16/1
MKL26Z64VFM4	64 KB	8 KB	32	QFN	23	19/4	7/0
MKL26Z64VFT4	64 KB	8 KB	48	QFN	36	24/4	14/1
MKL26Z64VLH4	64 KB	8 KB	64	LQFP	50	31/4	16/1
MKL27Z128VFM4	128 KB	32 KB	32	QFN	23	19/6	7/0
MKL27Z128VFT4	128 KB	32 KB	48	QFN	36	24/4	14/1
MKL27Z128VLH4	128 KB	32 KB	64	LQFP	50	31/6	16/2
MKL27Z128VMP4	128 KB	32 KB	64	MAPBGA	50	31/6	16/2
MKL27Z256VFM4	256 KB	32 KB	32	QFN	23	19/6	7/0
MKL27Z256VFT4	256 KB	32 KB	48	QFN	36	24/4	14/1
MKL27Z256VLH4	256 KB	32 KB	64	LQFP	50	31/6	16/2
MKL27Z256VMP4	256 KB	32 KB	64	MAPBGA	50	31/6	16/2
MKL27Z32VDA4	32 KB	8 KB	36	XFBGA	30	30/6	14/3
MKL27Z32VFM4	32 KB	8 KB	32	QFN[2]	24	24/6	8/0
MKL27Z32VFT4	32 KB	8 KB	48	QFN[2]	37	37/6	15/1
MKL27Z32VLH4	32 KB	8 KB	64	LQFP	51	51/6	17/2
MKL27Z32VMP4	32 KB	8 KB	64	MAPBGA[2]	51	51/6	17/2
MKL27Z64VDA4	64 KB	16 KB	36	XFBGA	30	30/6	14/3
MKL27Z64VFM4	64 KB	16 KB	32	QFN[2]	24	24/6	8/0
MKL27Z64VFT4	64 KB	16 KB	48	QFN[2]	37	37/6	15/1
MKL27Z64VLH4	64 KB	16 KB	64	LQFP	51	51/6	17/2
MKL27Z64VMP4	64 KB	16 KB	64	MAPBGA[2]	51	51/6	17/2
MKL28Z512VLL7	512 KB	128 KB	100	100LQFP	97	TBD	TBD

[1] INT: interrupt pin numbers; HD: high drive pin numbers

[2] This package is included in a Package Your Way program for Kinetis MCUs. Please visit www.nxp.com/KPYW for more detail.

11. Revision History

This table summarizes the changes made to this document since the initial release:

Table 5. Revision history

Revision	Date	Substantive changes
0	03/2015	Initial release
1	04/2016	Updated KL28

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