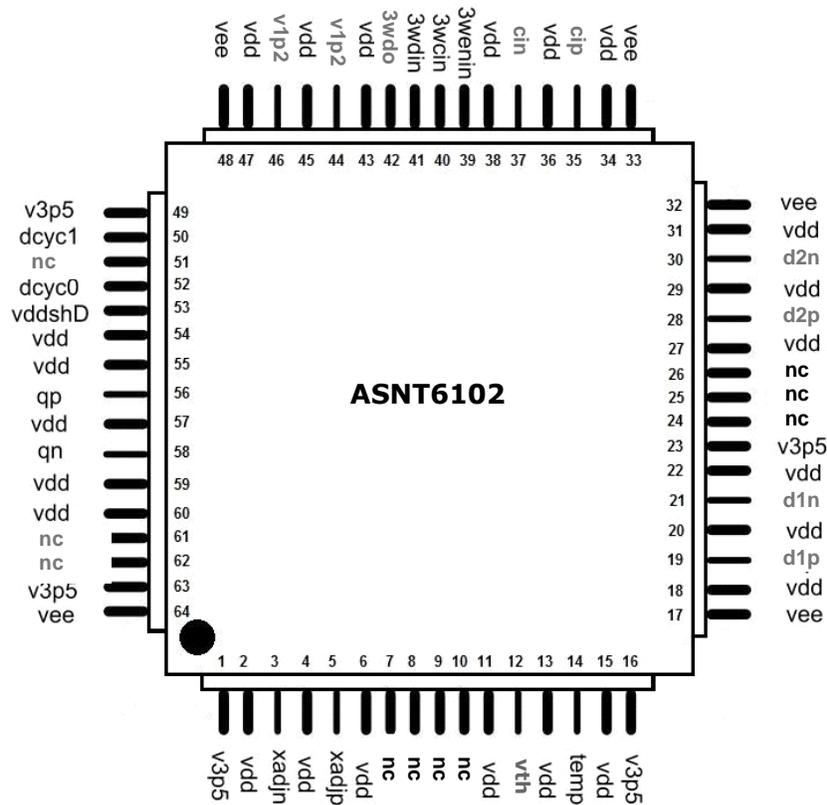




## ASNT6102-KMF 72Gbps-36Gbaud PAM4 Signal Generator/Encoder

- High-speed two input binary data signals to one PAM4 output signal
- Four pre-emphasis taps for each of 2 data channels with controlled weight and inversion
- Adjustable data output amplitude for all 3 levels and eye quality control
- Single-ended output data eye cross point adjustment
- Optional clock frequency multiplier by 2
- Main clock duty cycle indicators located before and after the multiplier
- Opposite and parallel adjustment of the main clock and data delays
- Fully differential CML input and output data, and clock interfaces
- 1.2V CMOS 3-wire interface for digital controls
- On-chip linear temperature sensor
- Two power supplies: negative -4.3V, floating positive +3.5V
- Maximum power consumption: 4.0W
- Power consumption depends on amplitude settings
- Custom CQFP 64-pin package







controlled through the SPI block as well. The SPI block is powered by internally generated supply voltage of +1.2V from **vee**. For more details see **3-Wire Interface Control Block**.

The internal clock signal that latches data in the sampling blocks is a copy of the input clock signal **cip/cin** with either matching or doubled (multiplied-by-2) frequency. In the multiply-by-2 clock mode, the duty cycles of the input and internal clock signals are monitored, and the output duty cycle can be adjusted through a designated control (see **Clock Multiplier**). For the part's correct operation, the input data rate in *Gbps* should be equal to the internal clock frequency in *GHz*.

Input clock and two data signals can be delayed independently by three control signals to ensure their correct phase relation at the inputs of the shift registers and at the chip outputs (see **Input Delay Section**).

The part's I/Os support CML logic interface with on-chip *50Ohm* termination to ground. External *50Ohm* termination is also required. DC-coupling for data and clock output ports is strongly recommended. The input ports can use DC or AC coupling. Differential connections of input clock and data are strongly recommended. Amplitude and peaking in data output signal can be adjusted. Both single-ended data output signals also have controlled eye crossing points (see **Data Output Buffer**).

The chip operates from one negative power supply (positive pin connected to external Ground,) and one floating positive power supply (negative pin connected to **vee** and positive pin **v3p5** = 3.5V). It is recommended to keep the relative deviation of **v3p5** from Ground within less than  $\pm 0.1V$ .

Additional supply voltage for internal CMOS circuitry is generated inside the chip or may be applied externally to pins **v1p2**.

## ***Input Delay Section***

As shown in Fig. 1, the encoder accepts two differential input data signals **d1p/d1n** and **d2p/d2n** as well as the clock signal **cip/cin**. The signals go through identical adjustable delay blocks **Adj. Delay**. Phase shifts of the three blocks are controlled independently by three digital bytes **skwadj1**, **skwadj2**, and **skwadjc** of the 3-wire interface block. The signals **skwadj1**, **skwadj2**, and **skwadjc** control the delays of the signals **d1p/d1n**, **d2p/d2n**, and **cip/cin** respectively.

## ***Clock Multiplier***

The clock multiplier **Clkx2** uses a "delay and XOR" mechanism to create output clock pulses from each edge of the input clock **cip/cin**. The multiplier is intended for operation with input clock signals within a certain frequency range specified in

**ELECTRICAL CHARACTERISTICS.** A 12-bit digital signal **ckdbradj** performs a dual function of multiplier activation and linear phase control. Voltages within the linear control range activate the multiplication function and are used for tuning the block's internal delay in order to achieve 50% duty cycle of the multiplied clock. The clock multiplier block may be turned off with the differential digital signal **byp/by**n. In order for the multiplier to turn off, **byp** bit should have the value of 1 and the **byn** bit should have the value of 0. When the clock multiplier is off, the delayed version of the input clock signal **cip/cin** is delivered to the sampling block with an unaltered frequency and an unaltered duty cycle. The opposite states of the **byp/by**n controls turn the multiplier on.



Two duty cycle control blocks DCycl are used for monitoring the clock pulse shapes before and after the multiplier. The first block is positioned before the multiplier and delivers single-ended analog voltage dcyc0 that indicates the input clock's duty cycle deviation from 50%. The second block is positioned after the multiplier and delivers a similar signal dcyc1 for the output clock. Both generated output voltages can be used in combination with ckbradj input within external control loops for getting an optimal shape of the multiplied clock.

## ***Sampling Block and Taps***

Sampling blocks SB1 and SB2 are 4-bit shift registers that generate 8 delayed data streams. The data streams T11, T12, T13, and T14 are the delayed versions of the input data signal d1p/d1n, MSB data. Similarly, the data streams T21, T22, T23, and T24 are the delayed versions of the input data signal d2p/d2n, LSB data. These data streams are needed for the 4-tap pre-emphasis capability. As stated above, the control bytes skwadj1, skwadj2, and skadjc are used to adjust the phase relationship between clock and data signals to ensure optimum sampling in both sampling blocks. The eight samples of the data streams with certain weights and polarities are delivered to the output and combined into a single analog differential output signal. The polarity of the data streams can be independently inverted with the digital control byte tapinv ("0"=direct, "1"=inverted) provided by the 3-wire interface.

## ***Data Output Buffer***

The 8 data streams from SB1 and SB2 are distributed among 12 identical parallel channels. Data is delivered through these channels to the output buffer. The output buffer consists of 12 identical open-collector buffers that deliver currents to two 50-Ohm resistors at the output. The resulting differential voltage on these resistors at the output of the chip represents a linear summation of all the taps. Twelve digital controls ochoff<1> through ochoff<12> can be used to turn any of the 12 channels on or off independently. If the control bit ochoff<X> has a value of 0, the channel X is on. If the control bit ochoff<X> has a value of 1, currents in two stages before the output stage are zero in channel X (where X is the number from 1 to 12), and the channel X does not pass data through. Shutting down unused channels before the output buffer stage reduces overall power consumption and minimizes cross-talk between taps.

Digital controls ochoff<1> through ochoff<12> do not affect currents in the 12 output buffers. The currents of the output buffers are linearly controlled through digital bytes tncl2 through tncl12 and DAC blocks. These controls can be used to independently adjust amplitudes of channels 2 through 12 from zero to maximum continuously in 256 steps (8-bit DAC). The amplitude of the output buffer of channel 1 is always at maximum, and cannot be adjusted. The only way to reduce the amplitude of channel 1 is to completely turn it off by using ochoff<1> control.

Digital controls pbxoff<2> through pbxoff<12> can be used to reduce currents in stages before output buffers in each channel to half of the maximum value. When the pbxoff<X> bit is 1, the amplitude of the buffer before the output stage in channel X is reduced by a factor of 2. Reducing the amplitude of this stage reduces peaking at the output at lower output amplitude settings which results in a cleaner output signal. Since the output amplitude of channel 1 is always at maximum the previous stage in channel 1 always has maximum amplitude which cannot be reduced.

As was mentioned earlier, 8 data streams (Tap11/12/13/14/21/22/23/24) from the sampling blocks are routed to 12 channel inputs of the output stage. After routing, data is retimed and is sent to the output



stage. The input of channel 1 is hardwired to Tap12. Each of inputs of other 11 channels may receive 1 of 2 tap data streams. The routing combinations depend on user-defined settings of digital controls  $ddr<2>$  through  $ddr<12>$ . The control bit  $ddr<X>$  determines which data stream is routed to the input of channel X. Table 1 presents tap assignment to channels depending on  $ddr<X>$  settings.

Table 1. Tap Assignment to Channels

Channel	$ddr<x>$	
	0	1
2	Tap12	Tap11
3	Tap12	Tap11
4	Tap12	Tap13
5	Tap12	Tap13
6	Tap13	Tap11
7	Tap12	Tap14
8	Tap22	Tap21
9	Tap22	Tap23
10	Tap22	Tap23
11	Tap23	Tap21
12	Tap22	Tap24

Since the currents of output stages of all the channels are added together the maximum weight of each tap at the output is determined by digital control settings of controls  $ddr<2>$  through  $ddr<12>$  and  $ocoff<1>$ . Table 2 presents all valid pre-emphasis combinations of maximum tap weights for MSB data input  $d1p/d1n$  along with the corresponding digital control settings.

Table 2. Maximum Tap Weight Combinations for MSB Data Stream

Tap11	Tap12	Tap13	Tap14	$ocoff<1>$	$ddr<2>$	$ddr<3>$	$ddr<4>$	$ddr<5>$	$ddr<6>$	$ddr<7>$
0	6	1	0	0	0	0	0	0	0	0
1	6	0	0	0	0	0	0	0	1	0
0	5	2	0	0	0	0	0	1	0	0
0	5	2	0	0	0	0	1	0	0	0
2	5	0	0	0	0	1	0	0	1	0
2	5	0	0	0	1	0	0	0	1	0
1	5	1	0	0	0	0	0	1	1	0
1	5	1	0	0	0	1	0	0	0	0
1	5	1	0	0	0	0	1	0	1	0
1	5	1	0	0	1	0	0	0	0	0
0	5	1	1	0	0	0	0	0	0	1
0	4	3	0	0	0	0	1	1	0	0
0	4	2	1	0	0	0	0	1	0	1
0	4	2	1	0	0	0	1	0	0	1
1	4	2	0	0	0	0	1	1	1	0
1	4	2	0	0	0	1	0	1	0	0
1	4	2	0	0	0	1	1	0	0	0
1	4	2	0	0	1	0	0	1	0	0
1	4	2	0	0	1	0	1	0	0	0
1	4	1	1	0	0	0	0	1	1	1



1	4	1	1	0	0	0	1	0	1	1
1	4	1	1	0	0	1	0	0	0	1
<b>Tap11</b>	<b>Tap12</b>	<b>Tap13</b>	<b>Tap14</b>	<b>ochoff&lt;1&gt;</b>	<b>ddr&lt;2&gt;</b>	<b>ddr&lt;3&gt;</b>	<b>ddr&lt;4&gt;</b>	<b>ddr&lt;5&gt;</b>	<b>ddr&lt;6&gt;</b>	<b>ddr&lt;7&gt;</b>
1	4	1	1	0	1	0	0	0	0	1
2	4	1	0	0	0	1	0	1	1	0
2	4	1	0	0	0	1	1	0	1	0
2	4	1	0	0	1	0	0	1	1	0
2	4	1	0	0	1	0	1	0	1	0
2	4	1	0	0	1	1	0	0	0	0
3	4	0	0	0	1	1	0	0	1	0
0	3	3	1	0	0	0	1	1	0	1
1	3	3	0	0	1	0	1	1	0	0
1	3	3	0	0	0	1	1	1	0	0
1	3	2	1	0	0	0	1	1	1	1
1	3	2	1	0	0	1	0	1	0	1
1	3	2	1	0	0	1	1	0	0	1
1	3	2	1	0	1	0	0	1	0	1
1	3	2	1	0	1	0	1	0	0	1
2	3	2	0	0	0	1	1	1	1	0
2	3	2	0	0	1	0	1	1	1	0
2	3	2	0	0	1	1	0	1	0	0
2	3	2	0	0	1	1	1	0	0	0
2	3	1	1	0	0	1	0	1	1	1
2	3	1	1	0	0	1	1	0	1	1
2	3	1	1	0	1	0	0	1	1	1
2	3	1	1	0	1	0	1	0	1	1
2	3	1	1	0	1	1	0	0	0	1
3	3	1	0	0	1	1	0	1	1	0
3	3	1	0	0	1	1	1	0	1	0
2	2	3	0	0	1	1	1	1	0	0
1	2	3	1	0	0	1	1	1	0	1
1	2	3	1	0	1	0	1	1	0	1
3	2	1	1	0	1	1	0	1	1	1
3	2	1	1	0	1	1	1	0	1	1
3	2	2	0	0	1	1	1	1	1	0
2	2	2	1	0	0	1	1	1	1	1
2	2	2	1	0	1	0	1	1	1	1
2	2	2	1	0	1	1	0	1	0	1
2	2	2	1	0	1	1	1	0	0	1
0	5	1	0	1	0	0	0	0	0	0
1	5	0	0	1	0	0	0	0	1	0
0	4	2	0	1	0	0	0	1	0	0
0	4	2	0	1	0	0	1	0	0	0
0	4	1	1	1	0	0	0	0	0	1
1	4	1	0	1	0	0	0	1	1	0
1	4	1	0	1	0	0	1	0	1	0
1	4	1	0	1	0	1	0	0	0	0
1	4	1	0	1	1	0	0	0	0	0



2	4	0	0	1	0	1	0	0	1	0
2	4	0	0	1	1	0	0	0	1	0
<b>Tap11</b>	<b>Tap12</b>	<b>Tap13</b>	<b>Tap14</b>	<b>ochoff&lt;1&gt;</b>	<b>ddr&lt;2&gt;</b>	<b>ddr&lt;3&gt;</b>	<b>ddr&lt;4&gt;</b>	<b>ddr&lt;5&gt;</b>	<b>ddr&lt;6&gt;</b>	<b>ddr&lt;7&gt;</b>
0	3	3	0	1	0	0	1	1	0	0
0	3	2	1	1	0	0	0	1	0	1
0	3	2	1	1	0	0	1	0	0	1
1	3	2	0	1	0	0	1	1	1	0
1	3	2	0	1	0	1	0	1	0	0
1	3	2	0	1	0	1	1	0	0	0
1	3	2	0	1	1	0	0	1	0	0
1	3	2	0	1	1	0	1	0	0	0
1	3	1	1	1	0	0	0	1	1	1
1	3	1	1	1	0	0	1	0	1	1
1	3	1	1	1	0	1	0	0	0	1
1	3	1	1	1	1	0	0	0	0	1
2	3	1	0	1	0	1	0	1	1	0
2	3	1	0	1	0	1	1	0	1	0
2	3	1	0	1	1	0	0	1	1	0
2	3	1	0	1	1	1	0	0	0	0
2	3	1	0	1	1	1	0	0	0	0
3	3	0	0	1	1	1	0	0	1	0
0	2	3	1	1	0	0	1	1	0	1
1	2	3	0	1	0	1	1	1	0	0
1	2	3	0	1	1	0	1	1	0	0
1	1	3	1	1	0	1	1	1	0	1
1	1	3	1	1	1	0	1	1	0	1
1	2	2	1	1	0	0	1	1	1	1
1	2	2	1	1	0	1	0	1	0	1
1	2	2	1	1	0	1	1	0	0	1
1	2	2	1	1	1	0	0	1	0	1
1	2	2	1	1	1	0	1	0	0	1
2	2	1	1	1	0	1	0	1	1	1
2	2	1	1	1	0	1	1	0	1	1
2	2	1	1	1	1	0	1	0	1	1
2	2	1	1	1	1	1	0	0	0	1
2	2	2	0	1	0	1	1	1	1	0
2	2	2	0	1	1	0	1	1	1	0
2	2	2	0	1	1	1	0	1	0	0
2	2	2	0	1	1	1	1	0	0	0
2	2	2	0	1	1	1	1	0	0	0
3	2	1	0	1	1	1	0	1	1	0
3	2	1	0	1	1	1	1	0	1	0
3	1	1	1	1	1	1	0	1	1	1
3	1	1	1	1	1	1	1	0	1	1

When the control **ochoff<1>** is 0, channel 1 is on. The amplitude of channel 1, which is always connected to **Tap12**, cannot be lowered through analog controls. Other tap weights can be lowered to zero through analog controls **tncriX**. As a result, if **ochoff<1>** is 0, **Tap12** is always present at the output with the



minimum weight of 1. If `ochoff<1>` is 1, then the weight of each tap can be set to any fraction of full weight between zero and the maximum value presented in the table.

Table 3 presents all valid pre-emphasis combinations of maximum tap weights for LSB data input `d2p/d2n` along with the corresponding digital control settings.

Table 3. Maximum Tap Weight Combinations for LSB Data Stream

Tap21	Tap22	Tap23	Tap24	ddr<8>	ddr<9>	ddr<10>	ddr<11>	ddr<12>
0	4	1	0	0	0	0	0	0
1	4	0	0	0	0	0	1	0
0	3	2	0	0	0	1	0	0
0	3	2	0	0	1	0	0	0
0	3	1	1	0	0	0	0	1
1	3	1	0	0	0	1	1	0
1	3	1	0	0	1	0	1	0
1	3	1	0	1	0	0	0	0
2	3	0	0	1	0	0	1	0
0	2	3	0	0	1	1	0	0
1	1	3	0	1	1	1	0	0
0	1	3	1	0	1	1	0	1
0	2	2	1	0	0	1	0	1
0	2	2	1	0	1	0	0	1
1	2	2	0	0	1	1	1	0
1	2	2	0	1	0	1	0	0
1	2	2	0	1	1	0	0	0
1	2	1	1	0	0	1	1	1
1	2	1	1	0	1	0	1	1
1	2	1	1	1	0	0	0	1
2	2	1	0	1	1	0	1	0
1	1	2	1	0	1	1	1	1
1	1	2	1	1	0	1	0	1
1	1	2	1	1	1	0	0	1
2	2	1	0	1	0	1	1	0
2	2	1	0	1	1	0	1	0
2	1	1	1	1	0	1	1	1
2	1	1	1	1	1	0	1	1

The weight of each tap for LSB data stream can be set to any fraction of full weight between zero and the maximum value presented in the table.

Weight settings for MSB data and LSB data streams are independent of each other. In order to form a PAM4 signal the combined weight of the LSB taps should be equal to half of the combined weight of the MSB taps.

The quality of the output signal shape can be optimized using the digital control byte `vshcrID`. An internal DAC block provides an analog signal that controls the voltage on bases of cascode transistors of output buffers. Higher values of the digital control code `vshcrID` correspond to lower values of the voltage. This

voltage controls peaking on the falling edge of the output signal. More positive voltages correspond to higher peaking. This voltage can be monitored and adjusted through an external pin `vddshD`. The internal common-mode level reference voltage for analog amplitude control of all output buffers can be adjusted through the control byte `vtocr1`. Maximum or minimum amplitude settings may be adjusted with this control for all output buffers simultaneously. Differential analog control voltage `xadjp/xadjn` can be utilized to adjust the crossing points of single-ended output eyes. At the default state of `xadjp = xadjn = 0V`, the crossing points in both direct and inverted eyes should be centered. The crossing points are moving up in the direct eye and down in the inverted eye if  $xadjp = -xadjn > 0$ , or in the opposite directions if  $xadjp = -xadjn < 0$ .

An example of the PAM4 output eye at 32GBaud is shown in Fig. 2.

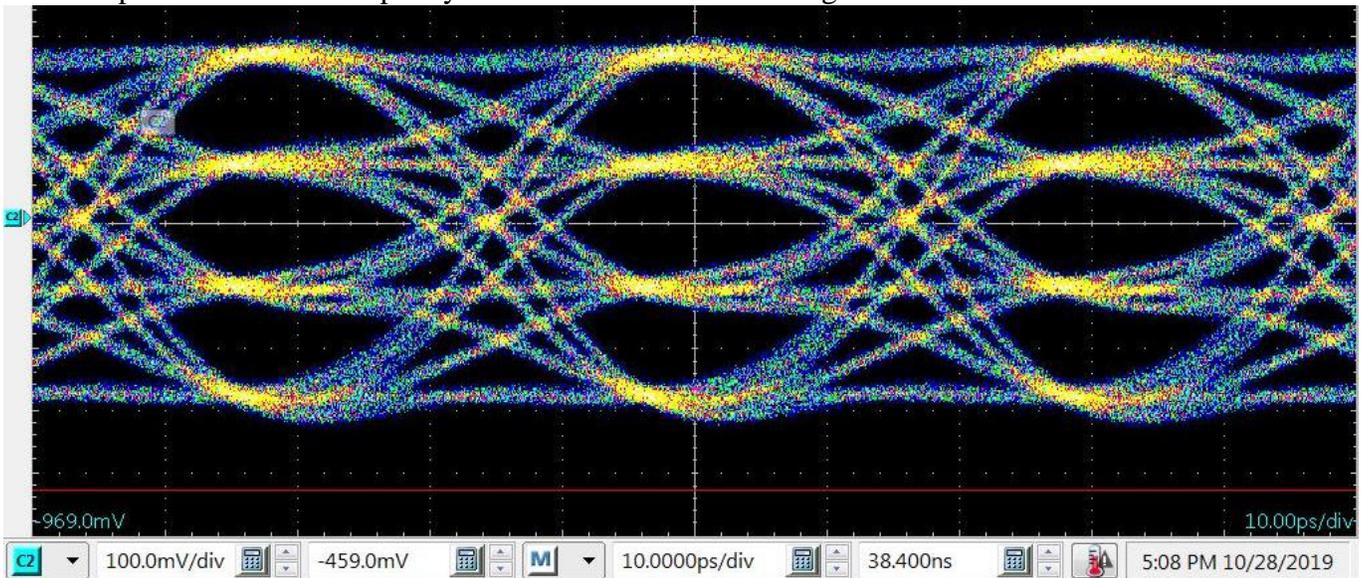


Fig. 2. PAM4 Output Eye at 25GBaud

## Temperature Sensor

A linear temperature sensor is included on chip. Its behavior is illustrated in Fig. 3 below. The demonstrated voltage has been generated on the internal 11KOhm resistor connected to vdd.

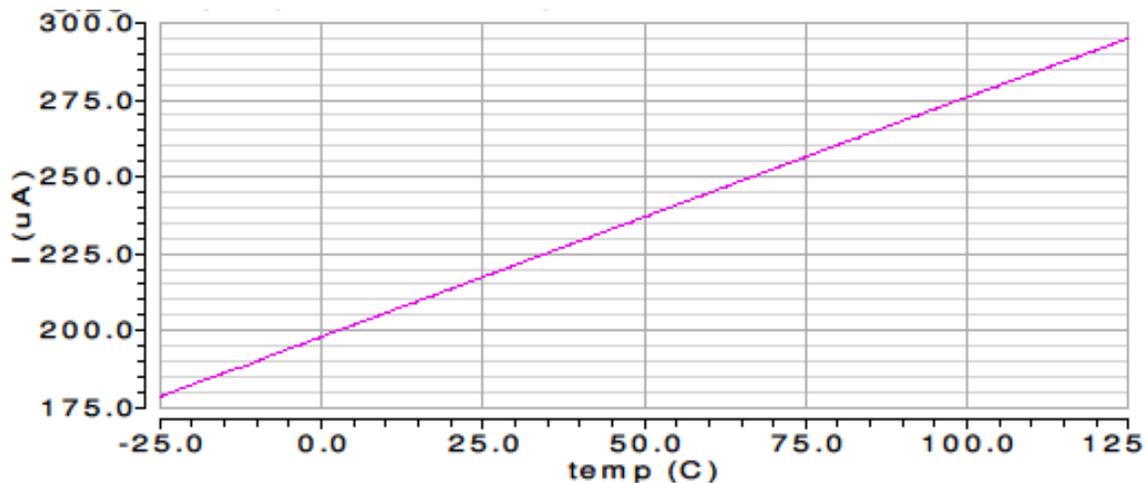




Fig. 3. Temperature Sensor's Characteristic

## 3-Wire Interface Control Block

To reduce the physical number of digital control inputs to the encoder chip, a 27-byte shift register with a 3-wire input interface has been included on chip. The SPI block is powered by internally generated supply voltage of +1.2V from **vee**. External pins **v1p2** can be used for monitoring and adjustment (if needed) of the internal power supply voltage of the SPI block. for normal operation, the pins **v1p2** should be left not connected. The digital control bits applied through **3wdin** input are latched in and shifted down the register with the low-speed clock **3wcin**. Write enable signal **3wenin** must be set to logic "1" during the data read-in phase. The SPI data can be monitored through the output **3wdo**. Table 4 presents the byte order of the 3-wire interface block.

Table 4. Control Bytes

Byte Number	Bit Number							
	7	6	5	4	3	2	1	0
1	skwadj1(7:0)							
2	skwadj2(7:0)							
3	skwadjc(7:0)							
4	ckdbrby[p/n]	offckob(NC)*	X	X	ckdbradj(11:8)			
5	ckdbradj(7:0)							
6	vgcC(7:0) (NC)							
7	vshcr1C(7:0) (NC)							
8	vthcr1(7:0)							
9	X	X	X	X	X	ddcr1(12:10)		
10	ddcr1(9:2)							
11	X	X	X	X	ochoff(12:9)			
12	ochoff(8:1)							
13	X	X	X	X	X	pbxoff(12:10)		
14	pbxoff(9:2)							
15	tapinv(8:1)							
16	tncr12(7:0)							
17	tncr13(7:0)							
18	tncr14(7:0)							
19	tncr15(7:0)							
20	tncr16(7:0)							
21	tncr17(7:0)							
22	tncr18(7:0)							
23	tncr19(7:0)							
24	tncr110(7:0)							
25	tncr111(7:0)							
26	tncr112(7:0)							
27	vshcr1D(7:0)							

\*) - these control bits and bytes are not used in the chip and should be kept at "0"

SPI load order is illustrated in Fig. 4.

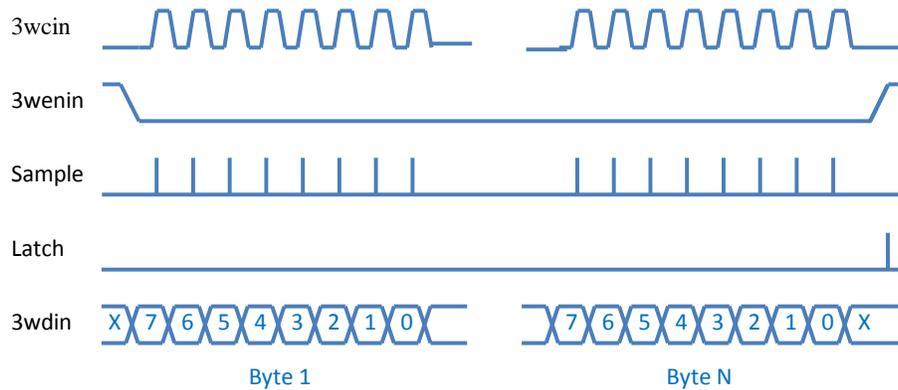


Fig. 4. SPI Load Order

## POWER SUPPLY CONFIGURATION

The part operates with a floating supply configuration shown in Fig. 5. The first negative supply (PSU1 source) is referenced to **vdd**, which is assumed to be the external ground (GND). Its negative pin provides the chip's internal common node voltage. The second supply (PSU2) is floating (not connected to GND) and has its negative pin connected to the negative pin of PSU1 (**vee**) and thus to the on-chip common node. The second power supply unit PSU2 provides a floating positive supply voltage **v3p5** for the high-speed internal circuitry. The third positive supply voltage **v1p2** for the internal CMOS circuitry is generated inside the chip but also can be supplied from outside using a third power supply unit PSU3 as shown in Fig. 5.

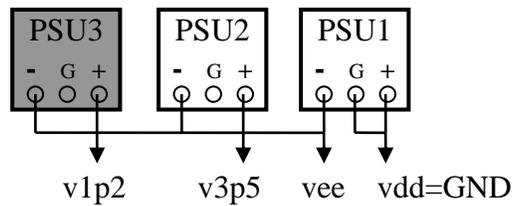


Fig. 5. Floating Supply Configuration

The part's output signals are referenced to **vdd**. If a different output reference voltage is required, **vdd** can be changed to any voltage. In this case, a fourth power supply is required and all other power supplies should be floating. For more details see the AN\_ASNT6102-KMM document.

**All the characteristics detailed below assume vdd=GND = 0.0V.**

## ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 5 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed **vdd**).



Table 5. Absolute Maximum Ratings

Parameter	Min	Max	Units
Negative Supply Voltage (vee)		-4.8	V
Positive Supply Voltage (v3p5)		3.8	V
Positive Supply Voltage (v1p2)		1.4	V
Power Consumption		5.0	W
RF Input Voltage Swing (SE)		1.2	V
Case Temperature		+90	°C
Storage Temperature	-40	+100	°C
Operational Humidity	10	98	%
Storage Humidity	10	98	%

## TERMINAL FUNCTIONS

TERMINAL			Description
Name	No.	Type	
<b>High-Speed I/Os</b>			
d1p	19	CML input with internal SE 50Ohm termination to VCC	Differential high-speed data input
d1n	21		
d2p	28		Differential high-speed data input
d2n	30		
cip	35		Differential high-speed clock input
cin	37		
qp	56	CML output requires external SE 50Ohm termination to VCC	Differential high-speed clock output
qn	58		
<b>Low-Speed I/Os</b>			
3wenin	39	1.2V CMOS input	Enable input signal for 3-wire interface
3wcin	40		Clock input signal for 3-wire interface
3wdin	41		Data input signal for 3-wire interface
3wdo	42	1.2V CMOS output	Data output signal of 3-wire interface
<b>Analog Control Voltage Inputs</b>			
xadjp	5	Analog input	Output data eye cross point adjustment, Differential
xadjn	3		
vth	12		Internal reference voltage for analog amplitude adjustment of output buffers
<b>Analog Control Indicators</b>			
temp	14	Analog output	Linear temperature-dependent voltage output with internal 11KOhm termination to vdd.
dcyc1	50		Linear voltage indicating output clock duty cycle
dcyc0	52		Linear voltage indicating main input clock duty cycle



Supply And Termination Voltages		
Name	Description	Pin Number
vdd	External ground	2, 4, 6, 11, 13, 15, 18, 20, 22, 27, 29, 31, 34, 36, 38, 43, 45, 47, 54, 55, 57, 59, 60
vee	-4.3V negative power supply	17, 32, 33, 48, 64
v3p5	+3.5V positive power supply, negative pin to vee	1, 16, 23, 49, 63
v1p2	+1.2V positive power supply, negative pin to vee. Generated inside the chip	44, 46
vddshD	Output data peaking adjustment positive power supply. Negative pin to vee	53
nc	Not connected	7, 8, 9, 10, 24, 25, 26, 51, 61, 62

## ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>Variable supply voltages (vddshd)</b>					
Voltage range	2.8		4.3	V	“-“ pin to vee
$I_{vddshd}$		2.2		mA	All 4 taps active
<b>Duty Cycle Indicator (dcyc0/dcyc1)</b>					
Voltage range	vdd-3.3		vdd-0.8	V	
<b>Temperature Sensor (temp)</b>					
Voltage range	vdd-3.3		vdd-2.3	V	
<b>3-Wire Inputs (3wdin, 3wcin, 3wenin)</b>					
High voltage level	vdd-0.2		vdd	V	
Low voltage level	vdd-1.4		vdd-1.2	V	
Clock speed		350	400	MHz	

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
<b>General Parameters</b>					
vee	-4.1	-4.3	-4.5	V	
vdd		0.0		V	External ground
v3p5	3.4	3.5	3.6	V	“-“ pin to vee
$I_{4.3}$	120		220	mA	Depending on the settings data amplitudes <sup>1)</sup>
$I_{v3p5}$	850		1020	mA	
Power	3.5	4.0	4.5	W	
Junction temperature	0	50	100	°C	
<b>Data input (d1p/d1n, d2p/d2n)</b>					
Rate	1.0		36	Gb/s	
SE Swing	50	200	500	mV	Peak-to-peak
CM Level	vdd-(SE swing)/2				



Clock inputs (cip/cin)					
Frequency (Ci input)	1.0	16	GHz	Fx1 mode	
	4.0	18	GHz	Fx2 mode, ckdbadj needs tuning	
SE Swing	50	200	500	mV	Peak-to-peak
CM Level	vdd-(SE swing)/2				
Data output (qp/qn)					
Rate	1.0	36	Gb/s		
SE Swing	0.0	1400	mV		Peak-to-peak
CM Level	vdd-0.1	vdd-0.70	V		Depends on the amplitude <sup>2)</sup>
Rise/Fall Times	12	13	14	ps	20%-80%
Cross point control (xadjp/xadjn)					
Differential voltage range	vdd-8.0	vdd+8.0	V		±4V at each input
CM Level	vdd				
Current in/out of the pin	+4 / -4		mA		at +4V / -4V
Threshold control (vth)					
Voltage range	vdd-.8	vdd	V		
PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Externally Controlled Operational Ranges					
Input Clock delay	0	+26		ps	
Input Data delay	0	+26		ps	
Output eye cross point	-25	+25		%	of the eye amplitude

## PACKAGE INFORMATION

The chip die is housed in a custom 64-pin CQFP package. The dimensioned drawings are shown in Fig. 6. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vdd plane, which is ground for a negative supply, or power for a positive supply.

The part's identification label is ASNT6102-KMF. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.



## 64-PIN KMF Package

All Dimensions are in millimeters

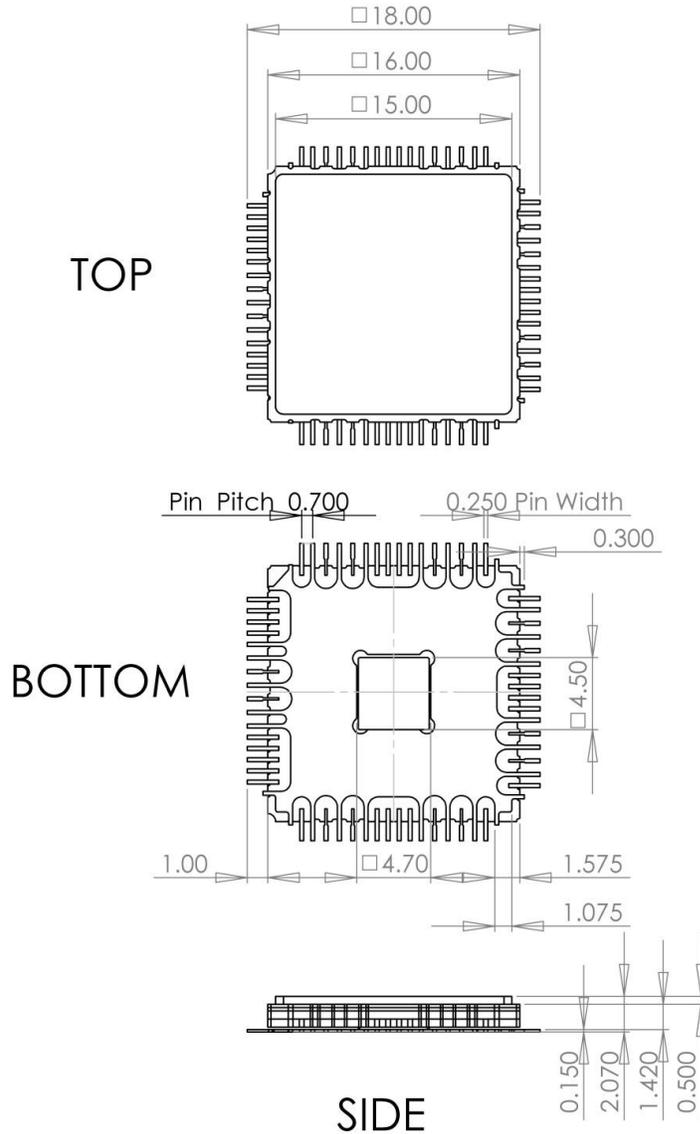


Fig. 6. CQFP 64-Pin Package Drawing (All Dimensions in mm)



## REVISION HISTORY

Revision	Date	Changes
1.2.2	02-2020	Updated Package Information
1.1.2	10-2019	Updated eye diagram
1.0.2	10-2019	Official release, removed PRELIMINARY mark Corrected title Corrected data rate values
0.0.2	07-2019	Updated header
0.0.1	01-2019	Preliminary release