

# NUD3048

## FET Switch

100 V, 800 mΩ, N-Channel, TSOP-6

The NUD3048 provides a single device solution for a number of applications requiring a low power, high voltage, FET switch. The package includes a gate resistor and gate to source zener clamp. This switch can accommodate a wide range of input voltages, making it compatible with most current logic levels. Its 100 V rating makes it compatible with 48 V telecom applications.

### Features

- 100 V Rating On Gate 2
- Integrated 100 k R<sub>G</sub> Option
- Integrated ESD Diode Protection
- Low Threshold Voltage
- Pb-Free Package is Available

### Typical Applications

- FET Switch
- Inverter
- Level Shifter
- Inrush Limiter
- Relay Driver

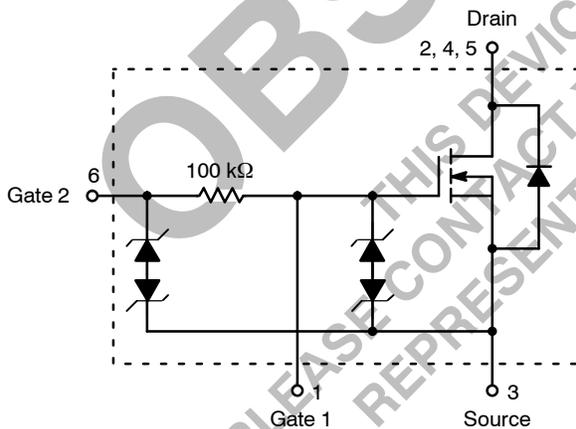


Figure 1. Block Diagram



ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM



JW7 = Specific Device Code

M = Month Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NUD3048MT1	TSOP-6	3000 / Tape & Reel
NUD3048MT1G	TSOP-6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NUD3048

## MAXIMUM RATINGS

Symbol	Rating	Value	Unit
$V_{DSS}$	Drain to Source Voltage – Continuous	100	V
$V_{G1SS}$	Gate to Source Voltage – Continuous @ 1.0 mA	15	V
$I_D$	Drain Current – Continuous ( $T_A = 25^\circ\text{C}$ ) (Note 1) (Note 2)	0.7 1.2	A
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) (Note 1) (Note 2)	0.66 1.56	W
$V_{G2SS}$	Gate Resistor to Source Voltage – Continuous	100	V
$T_{Jmax}$	Maximum Junction Temperature	150	$^\circ\text{C}$
$R_{\theta JA}$	Thermal Impedance (Junction-to-Ambient) (Note 1) Thermal Impedance (Junction-to-Ambient) (Note 2)	190 80	$^\circ\text{C/W}$
ESD	Human Body Model (HBM) Class 2	2000	V
	Machine Model Class A According to EIA/JESD22/A114 Specification	160	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain to Source Leakage Current ( $V_{DS} = 80\text{ V}$ , $V_{GS} = 0\text{ V}$ )	$I_{DSS}$	–	20	100	$\mu\text{A}$
Gate Body Leakage Current ( $V_{GS} = 10\text{ V}$ , $V_{DS} = 0\text{ V}$ ) ( $V_{GS} = 10\text{ V}$ , $V_{DS} = 0\text{ V}$ , $T_J = 125^\circ\text{C}$ )	$I_{GSS}$	–	3.0	10	$\mu\text{A}$
	$I_{GSS}$	–	6.0	20	$\mu\text{A}$
<b>ON CHARACTERISTICS</b>					
Gate Threshold Voltage ( $I_D = 1.0\text{ mA}$ )	$V_{GS}$	1.3	1.7	2.0	V
Drain to Source Resistance ( $V_{GS} = 4.5\text{ V}$ , $I_D = 100\text{ mA}$ )	$R_{DS(on)}$	–	0.65	0.82	$\Omega$
Drain to Source Resistance ( $V_{GS} = 10\text{ V}$ , $I_D = 100\text{ mA}$ )	$R_{DS(on)}$	–	0.6	0.72	$\Omega$
<b>DYNAMIC CHARACTERISTICS</b>					
Input Capacitance ( $V_{DS} = 5.0\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 10\text{ kHz}$ )	$C_{iss}$	–	135	–	pF
Output Capacitance ( $V_{DS} = 5.0\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 10\text{ kHz}$ )	$C_{oss}$	–	75	–	pF
Transfer Capacitance ( $V_{DS} = 5.0\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 10\text{ kHz}$ )	$C_{rss}$	–	26	–	pF
<b>GATE BIAS CHARACTERISTICS</b>					
Gate Resistor	$R_G$	75	100	125	$\text{k}\Omega$
Gate Zener Breakdown Voltage ( $I_Z = 1.0\text{ mA}$ ) (Note 3)	$V_Z$	15	17	–	V
Gate Zener Breakdown Voltage ( $I_Z = 3.0\text{ mA}$ ) (Note 4)		100	115	–	V

1. Min pad, 1 oz. Cu.
2. 1 inch pad, 1 oz Cu.
3. Measured from gate 1 to source.
4. Measured from gate 2 to source.

# NUD3048

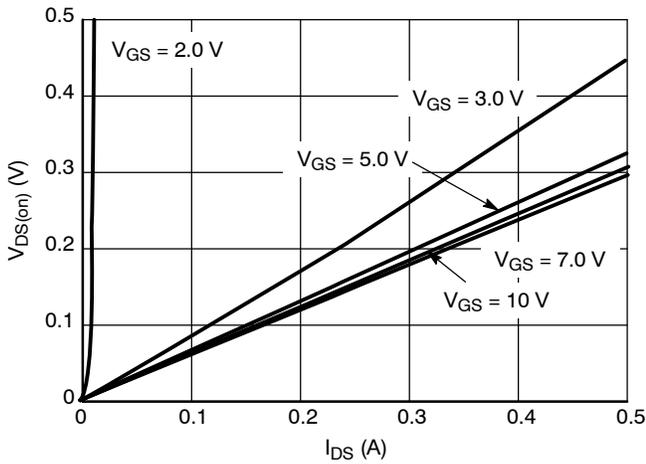


Figure 2.  $V_{DS(on)}$  Variation with  $I_{DS}$  and Gate Voltage

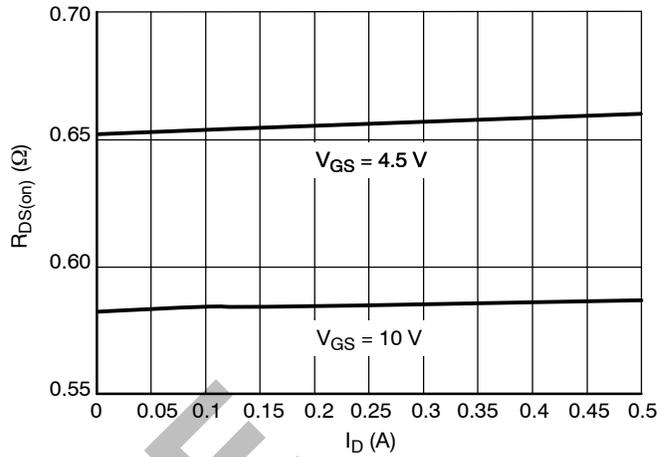


Figure 3. On Resistance Variation with Drain Current and Gate Voltage

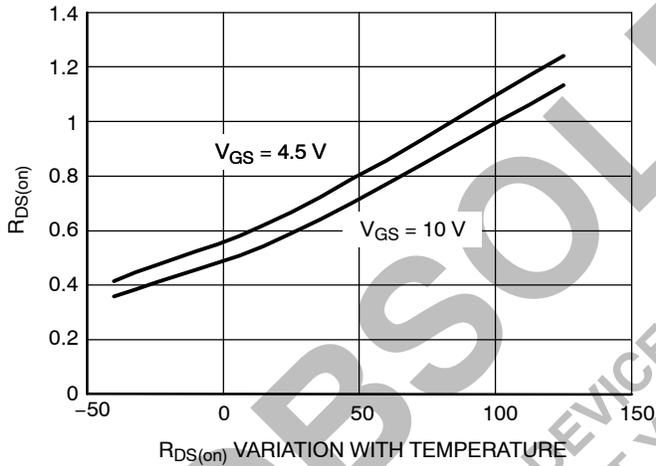


Figure 4. Variation of  $R_{DS(on)}$  with Temperature and Gate Voltage at  $I_D = 100$  mA

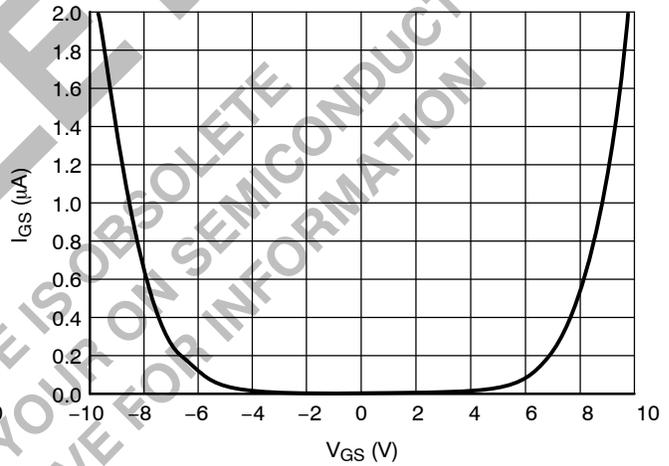


Figure 5. Gate Leakage Current Variation with Gate Voltage

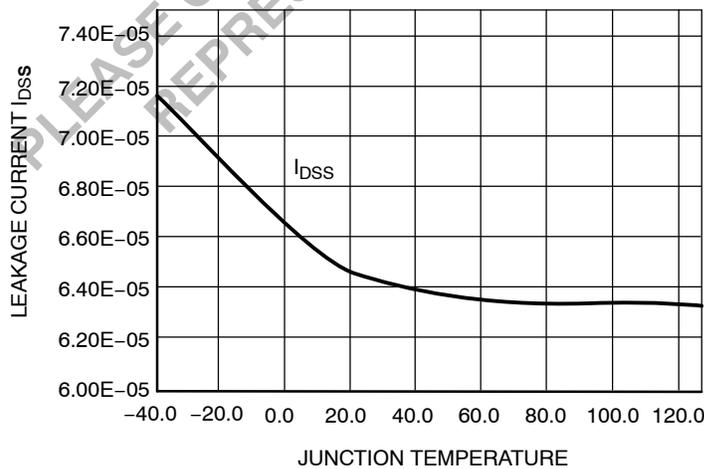
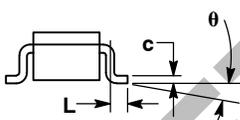
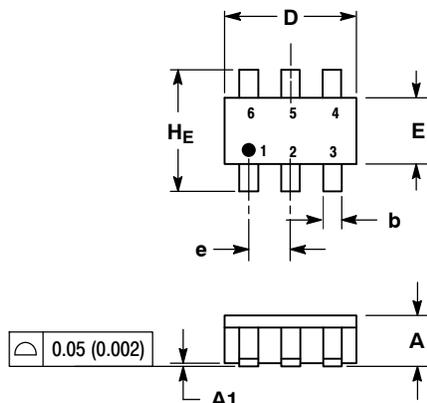


Figure 6. Variation of Leakage Current  $I_{DSS}$  (A) with  $V_{GS} = 0$  V and  $V_{DS} = 100$  V

# NUD3048

## PACKAGE DIMENSIONS

TSOP-6  
CASE 318G-02  
ISSUE P



NOTES:

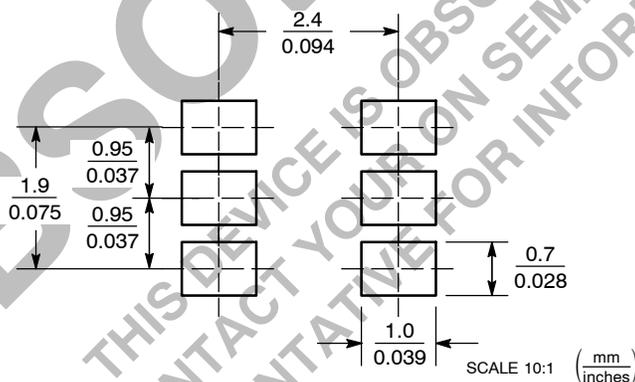
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.25	0.38	0.50	0.010	0.014	0.020
c	0.10	0.18	0.26	0.004	0.007	0.010
D	2.90	3.00	3.10	0.114	0.118	0.122
E	1.30	1.50	1.70	0.051	0.059	0.067
e	0.85	0.95	1.05	0.034	0.037	0.041
L	0.20	0.40	0.60	0.008	0.016	0.024
HE	2.50	2.75	3.00	0.099	0.108	0.118
θ	0°	-	10°	0°	-	10°

STYLE 9:

- PIN 1: LOW VOLTAGE GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN  
5. DRAIN  
6. HIGH VOLTAGE GATE

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada  
Europe, Middle East and Africa Technical Support:  
Phone: 421 33 790 2910  
Japan Customer Focus Center  
Phone: 81-3-5773-3850

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)  
Order Literature: <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative