

PE42524

Document Category: Product Specification

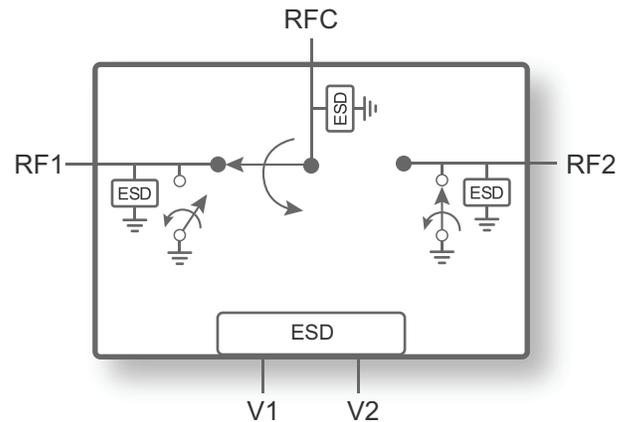
UltraCMOS® SPDT RF Switch, 10 MHz–40 GHz



Features

- Wideband support up to 40 GHz
- High port to port isolation
 - 48 dB @ 26.5 GHz
 - 39 dB @ 35 GHz
 - 33 dB @ 40 GHz
- Excellent linearity performance
 - P1dB of 31.5 dBm @ 26.5 GHz
 - P1dB of 28.0 dBm @ 35 GHz
 - IIP3 of 50 dBm @ 13.5 GHz
- Fast RF T_{rise}/T_{fall} time of 55 ns
- Low insertion loss
 - 1.8 dB @ 26.5 GHz
 - 3.1 dB @ 35 GHz
- Flip-chip die

Figure 1 • PE42524 Functional Diagram



Applications

- Test and measurement
- Microwave backhaul
- Radar
- Military communications

Product Description

The PE42524 is a HaRP™ technology-enhanced reflective SPDT RF switch die that supports a wide frequency range from 10 MHz to 40 GHz. This wideband flip-chip switch delivers high isolation performance, excellent linearity and low insertion loss, making this device ideal for test and measurement (T&M), microwave backhaul, radar and military communications (mil-comm) applications. At 30 GHz, the PE42524 exhibits 17 dB active port return loss, 47 dB isolation and 2.2 dB insertion loss. No blocking capacitors are required if DC voltage is not present on the RF ports.

The PE42524 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 ■ Absolute Maximum Ratings for PE42524

Parameter/Condition	Min	Max	Unit
Control voltage (V1, V2)	-3.5	3.5	V
RF input power (RFC–RFX, 50Ω)		Fig. 2	dBm
Storage temperature range	-65	+150	°C
ESD voltage HBM, all pins ^(*)		2000	V
Note: * Human body model (MIL-STD883 Method 3015).			

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for PE42524. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 ■ Recommended Operating Condition for PE42524

Parameter	Min	Typ	Max	Unit
Control high (V1, V2)	3.1	3.3	3.5	V
Control low (V1, V2)	-3.5	-3.3	-3.1	V
Control current		2		nA
RF input power, CW (RFC–RFX) ⁽¹⁾			Fig. 2	dBm
RF input power, pulsed (RFC–RFX) ⁽²⁾			Fig. 2	dBm
Operating temperature range	-40	+25	+85	°C

Notes:
 1) 100% duty cycle, all bands, 50Ω.
 2) Pulsed, 5% duty cycle of 4620 μs period, 50Ω.

Electrical Specifications

Table 3 provides the PE42524 key electrical specifications @ 25 °C, V1 = +3.3V, V2 = -3.3V or V1 = -3.3V, V2 = +3.3V ($Z_S = Z_L = 50\Omega$), unless otherwise specified.

Table 3 ■ PE42524 Electrical Specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Operation frequency			10 MHz		40 GHz	As shown
Insertion loss	RFC–RFX	10 MHz		0.6	0.85	dB
		10 MHz–7.5 GHz		1.0	1.30	dB
		7.5–10 GHz		1.1	1.50	dB
		10–13.5 GHz		1.3	1.65	dB
		13.5–18 GHz		1.4	1.75	dB
		18–20 GHz		1.4	1.75	dB
		20–26.5 GHz		1.8	2.20	dB
		26.5–30 GHz		2.2	2.70	dB
		30–35 GHz		3.1	4.10	dB
		35–40 GHz		5.5	—	dB

Table 3 ■ PE42524 Electrical Specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Isolation	All paths	10 MHz	74	84		dB
		10 MHz–7.5 GHz	60	64		dB
		7.5–10 GHz	58	65		dB
		10–13.5 GHz	51	58		dB
		13.5–18 GHz	50	53		dB
		18–20 GHz	49	52		dB
		20–26.5 GHz	44	48		dB
		26.5–30 GHz	43	47		dB
		30–35 GHz	35	39		dB
		35–40 GHz	28	33		dB
Return loss (active port)	RFC–RFX	10 MHz		25		dB
		10 MHz–7.5 GHz		16		dB
		7.5–10 GHz		15		dB
		10–13.5 GHz		17		dB
		13.5–18 GHz		21		dB
		18–20 GHz		21		dB
		20–26.5 GHz		18		dB
		26.5–30 GHz		17		dB
		30–35 GHz		14		dB
		35–40 GHz		6		dB
Return loss (RFC port)	RFC–RFX	10 MHz		25		dB
		10 MHz–7.5 GHz		18		dB
		7.5–10 GHz		19		dB
		10–13.5 GHz		26		dB
		13.5–18 GHz		29		dB
		18–20 GHz		23		dB
		20–26.5 GHz		31		dB
		26.5–30 GHz		30		dB
		30–35 GHz		16		dB
		35–40 GHz		7		dB
2nd harmonic, 2fo rejection	RFC–RFX	+25 dBm output power, 1 GHz		88		dBc
		+25 dBm output power, 6.5 GHz		84		dBc
		+25 dBm output power, 15 GHz		>89 ⁽¹⁾		dBc
Input 1dB compression point ⁽²⁾		10 MHz–40 GHz		Fig. 2		dBm
Input IP3		10–100 MHz		48		dBm
		1–2 GHz		50		dBm
		6–10 GHz		52		dBm
		10–13.5 GHz		50		dBm
Video feedthrough ⁽³⁾		DC measurement		3.5		mV _{PP}
RF T _{rise} /T _{fall}		10%/90% RF		55		ns
Settling time		50% CTRL to 0.05 dB final value		0.84	1.13	μs

Table 3 ■ PE42524 Electrical Specifications

Parameter	Path	Condition	Min	Typ	Max	Unit
Switching time		50% CTRL to 90% or 10% RF		225	304	ns

Notes:

- 1) Test system limited.
- 2) The input 1dB compression point is a linearity figure of merit. Refer to Table 2 for the RF input power (50Ω).
- 3) Measured with a 3.5 ns rise time, -3.3 / +3.3V pulse and 500 MHz bandwidth.

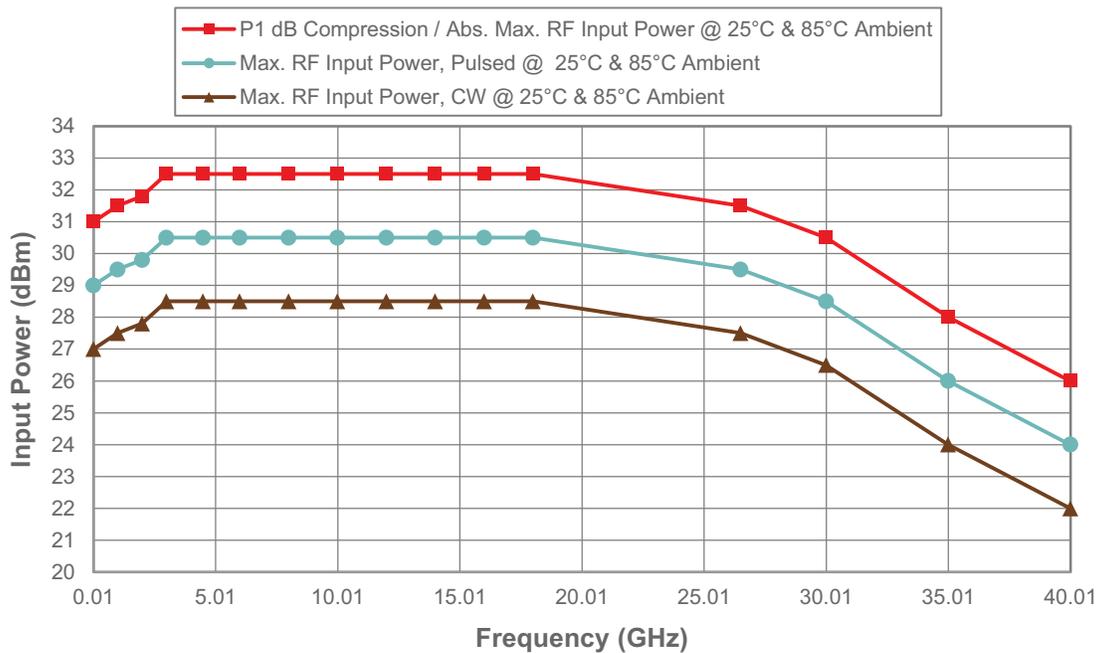
Control Logic

Table 4 provides the control logic truth table for the PE42524. States 2 and 3 are used in normal switching operations.

Table 4 ■ Truth Table for PE42524

V1	V2	RF1	RF2	State
-3.3V	-3.3V	OFF	OFF	1
-3.3V	+3.3V	OFF	ON	2
+3.3V	-3.3V	ON	OFF	3
+3.3V	+3.3V	ON	ON	4

Figure 2 ■ Power De-rating Curve (10 MHz–40 GHz) @ 25 °C and 85 °C Ambient (50?)



Typical Performance Data

Figure 3–Figure 12 show the typical performance data @ 25 °C, V1 = +3.3V, V2 = –3.3V, unless otherwise specified.

Figure 3 ■ Insertion Loss vs Temperature (RFC–RFX)

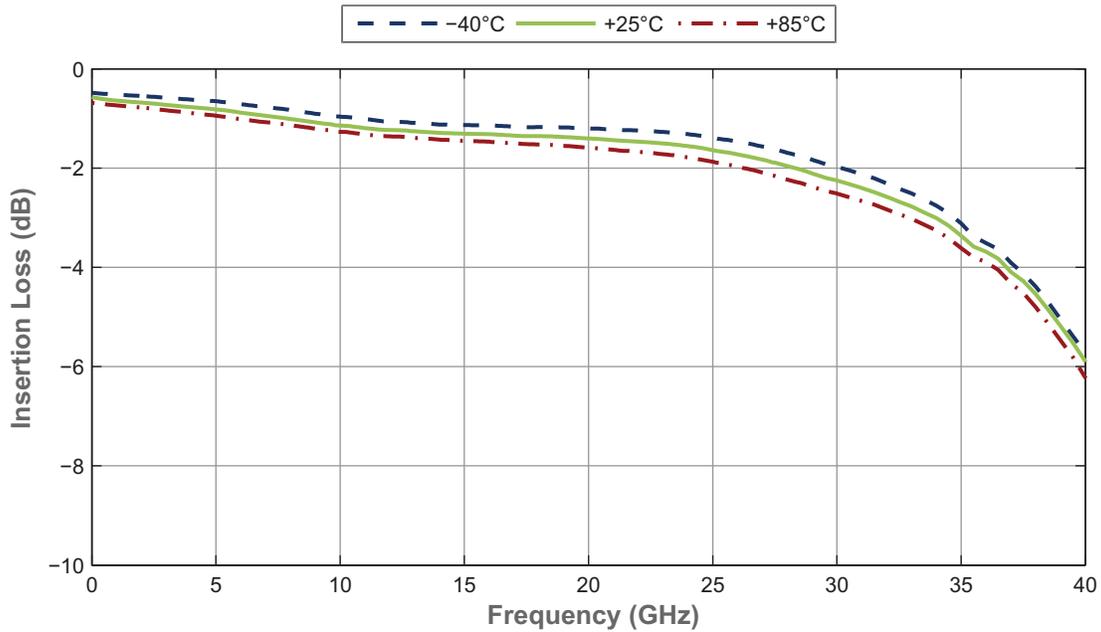


Figure 4 ■ Insertion Loss vs V1/V2 (RFC–RFX)

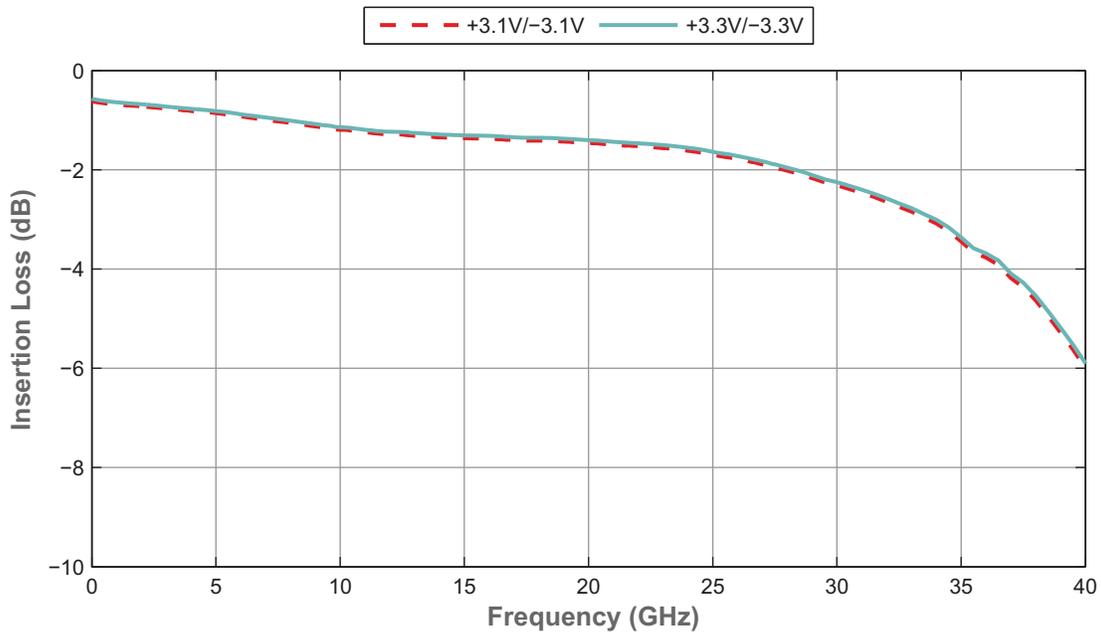


Figure 5 ■ RFC Port Return Loss vs Temperature

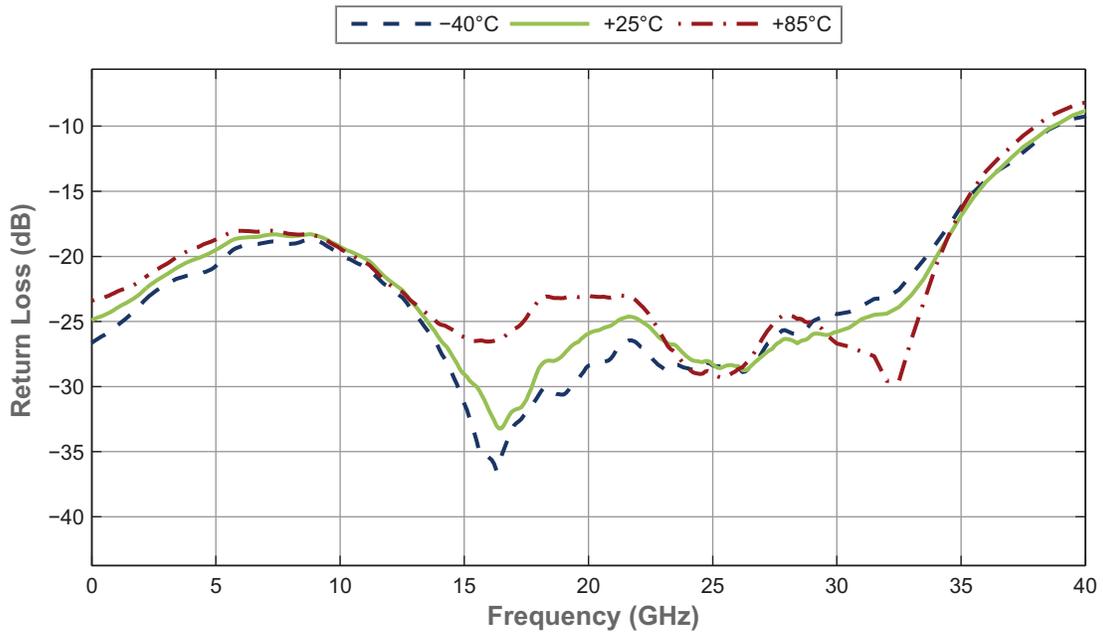


Figure 6 ■ RFC Port Return Loss vs V1/V2

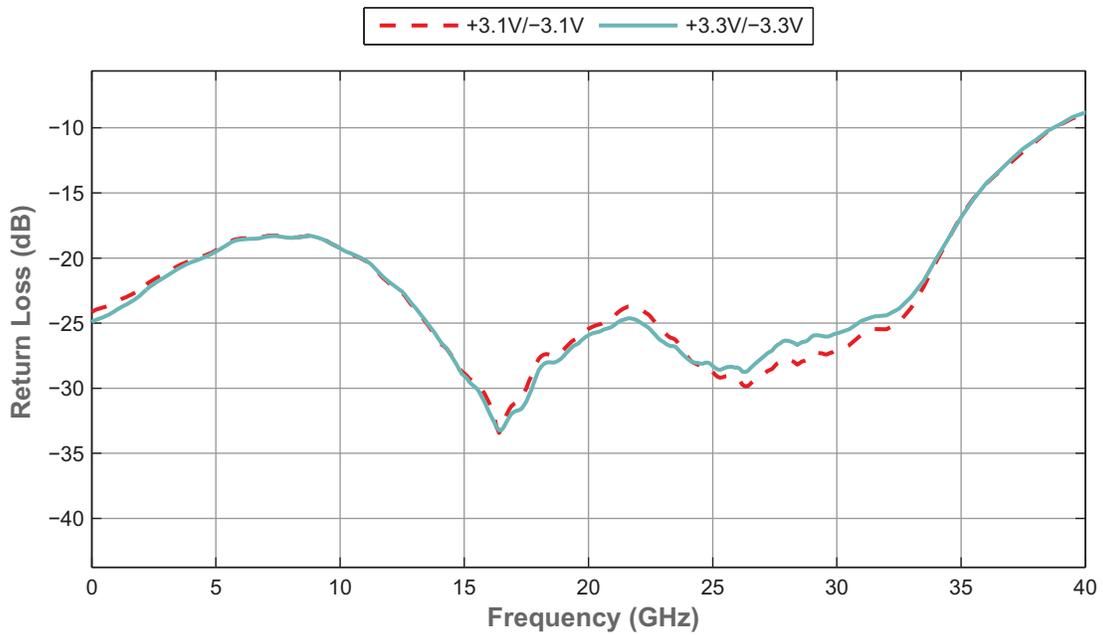


Figure 7 ■ Active Port Return Loss vs Temperature

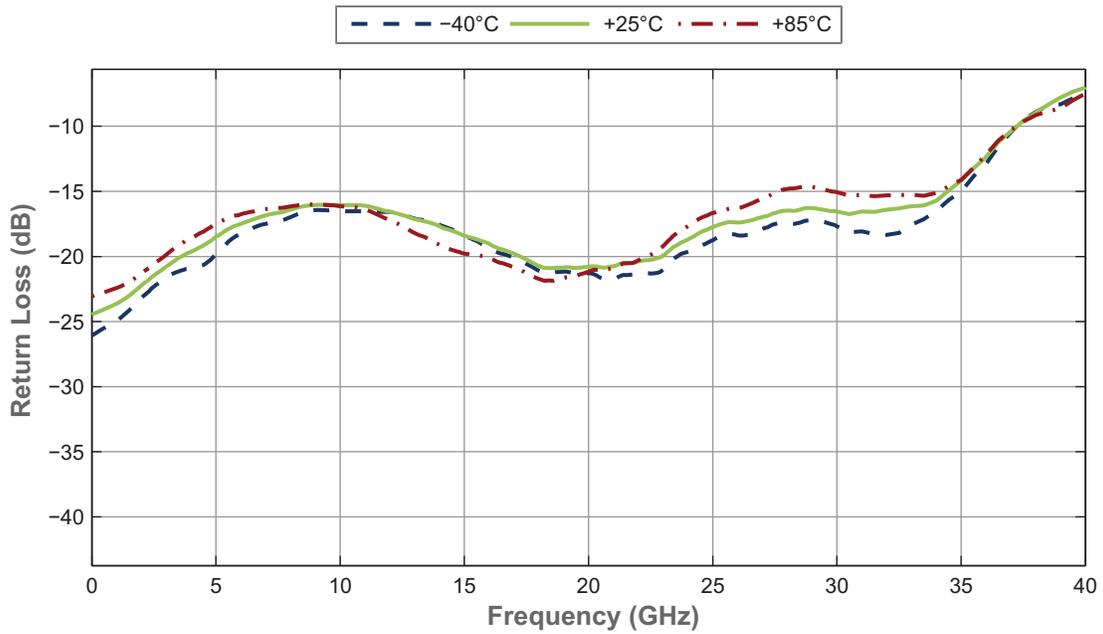


Figure 8 ■ Active Port Return Loss vs V1/V2

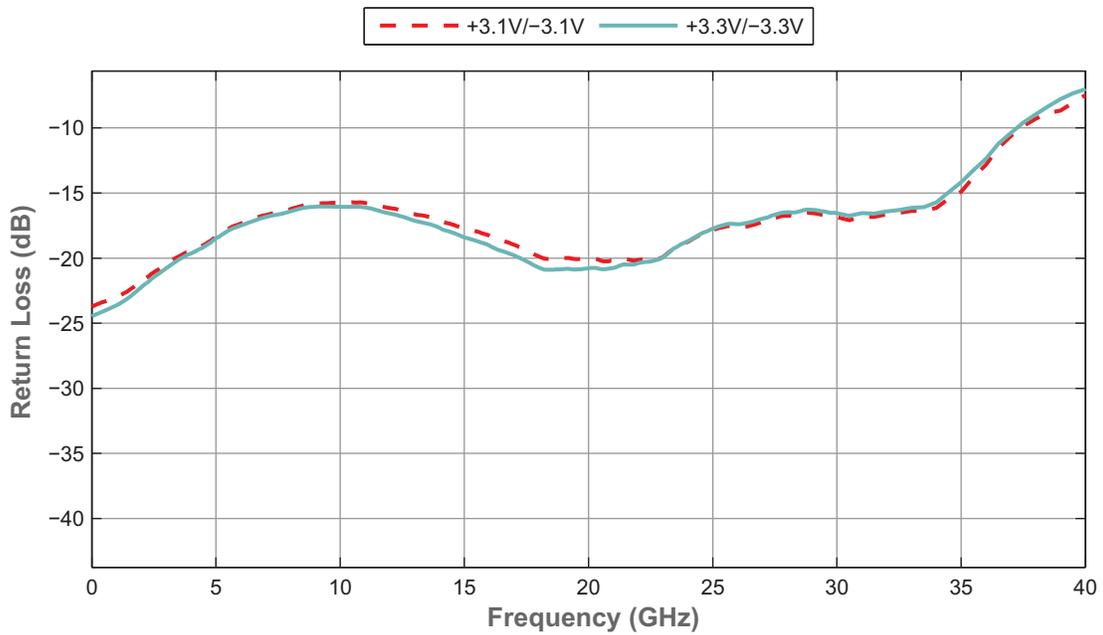


Figure 9 ■ Isolation vs Temperature (RFX-RFX)

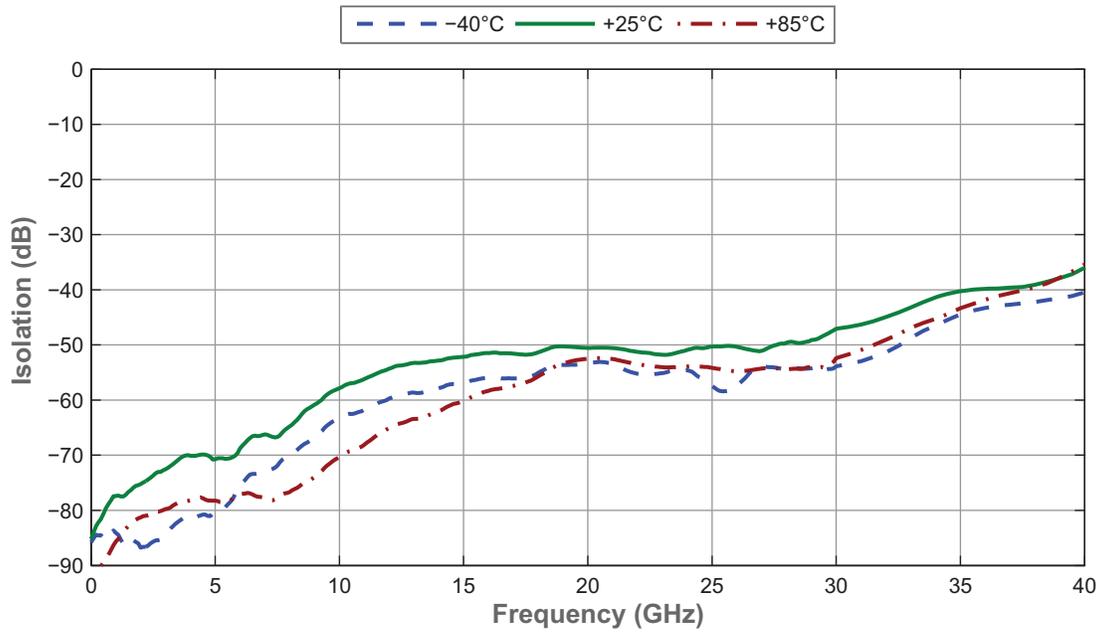


Figure 10 ■ Isolation vs V1/V2 (RFX-RFX)

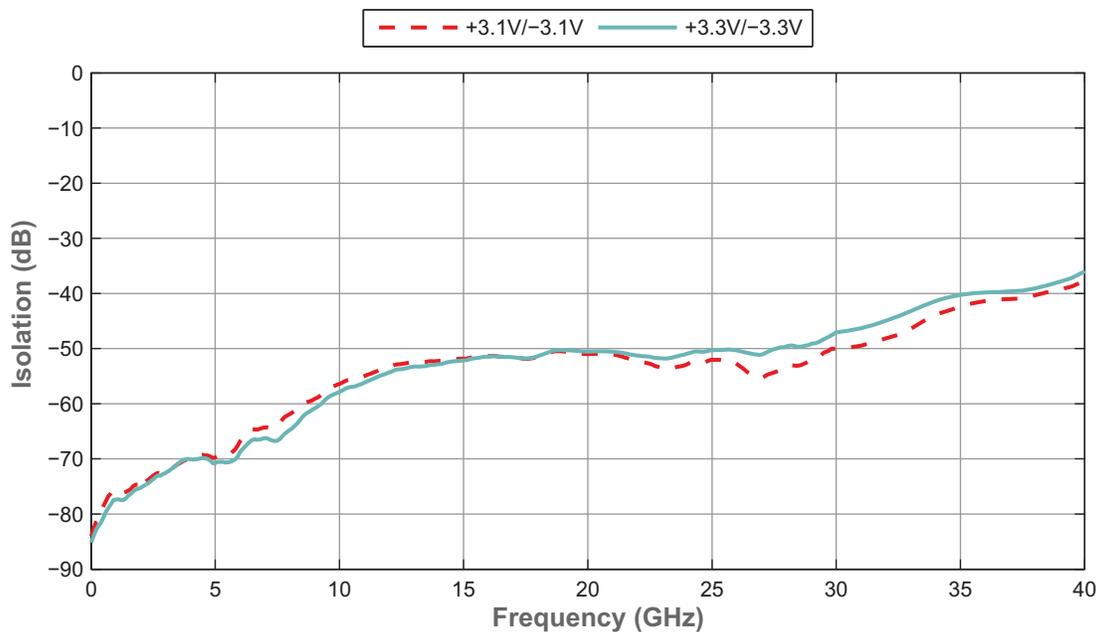


Figure 11 ■ Isolation vs Temperature (RFC–RFX)

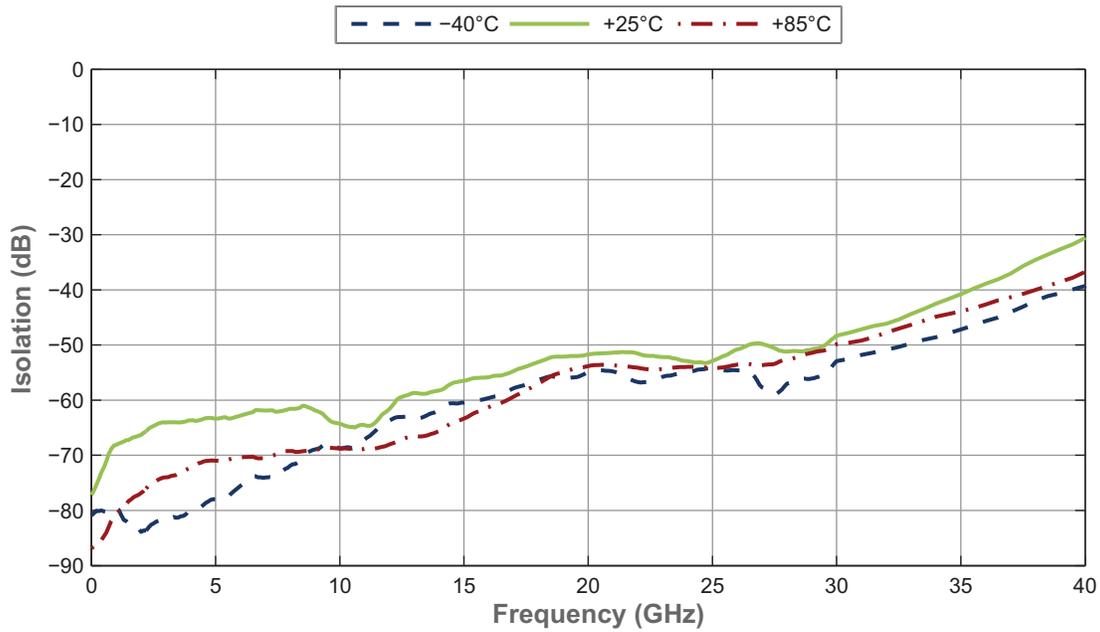
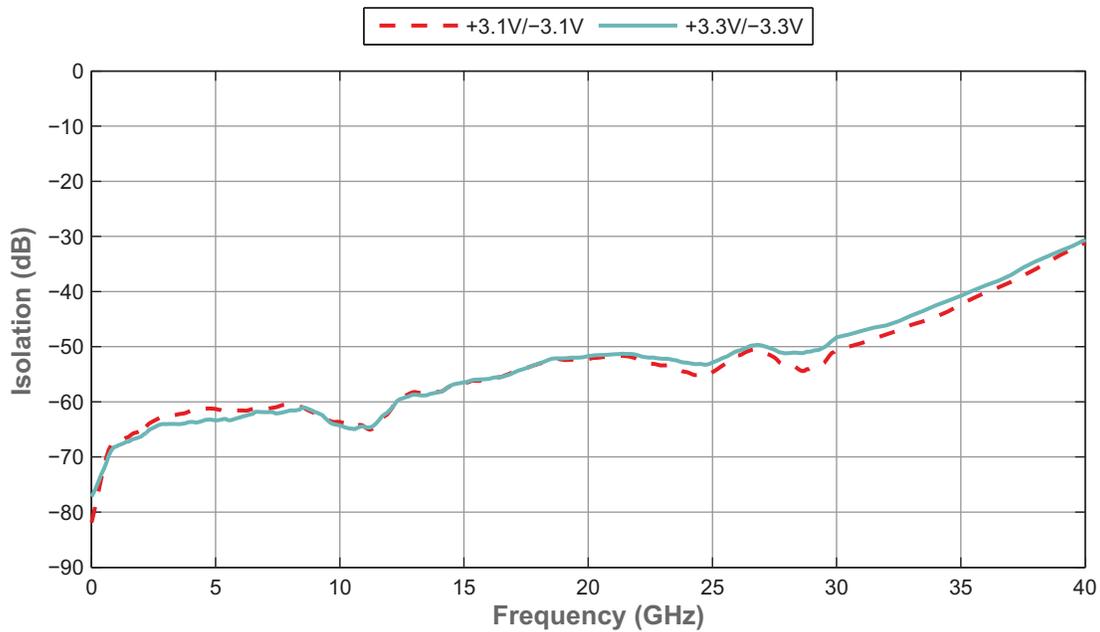


Figure 12 ■ Isolation vs V1/V2 (RFC–RFX)



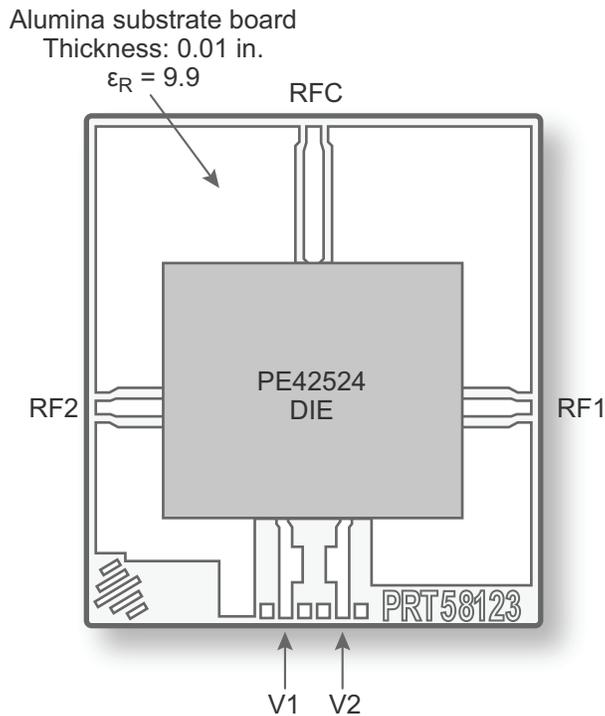
Recommended Evaluation Setup

The PE42524 s-parameter data and input 1dB compression point from 22–40 GHz (**Table 3** and **Figure 3–Figure 12**) were taken using grounded co-planar waveguide (CPWG) on the alumina substrate (shown in **Figure 13**) and RF probes.

The PE42524 2nd harmonic, 2fo rejection, input 1dB compression point below 18 GHz, input IP3 measurements, settling time and switching time (**Table 3**) were taken on a PCB using 2.92 mm connectors.

Bypass capacitors are not required.

Figure 13 ■ Alumina Substrate Board for PE42524



Pin Configuration

This section provides pin information for the PE42524. **Figure 14** shows the pin configuration of this device. **Table 5** provides a description for each pin.

Figure 14 ▪ Pin Configuration (Bumps Up) for PE42524

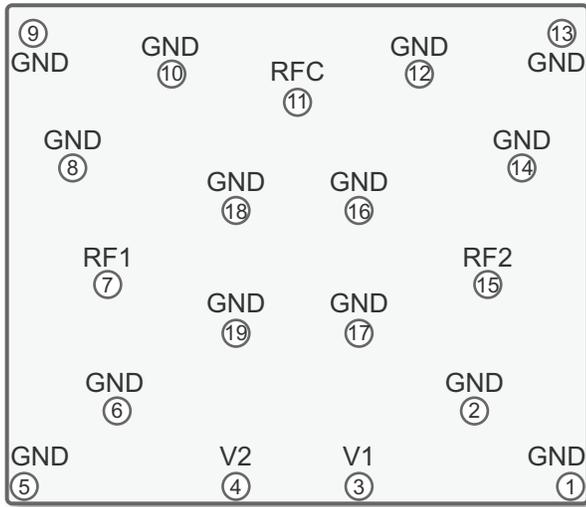


Table 5 ▪ Pin Descriptions for PE42524

Pin No.	Pin Name	Description
1, 2, 5, 6, 8–10, 12–14, 16–19	GND	Ground
7	RF1	RF port 1
11	RFC	RF common port
15	RF2	RF port 2
3	V1	Control input 1
4	V2	Control input 2

Die Mechanical Specifications

This section provides the die mechanical specifications for the PE42524.

Table 6 ■ *Mechanical Specifications for PE42524*

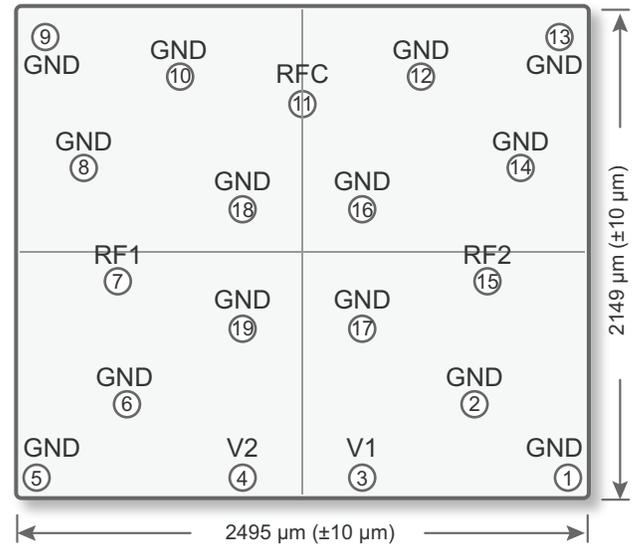
Parameter	Min	Typ	Max	Unit	Test Condition
Die size, singulated (x, y)	2466 × 2120	2486 × 2140	2516 × 2170	μm	Including excess sapphire, max. tolerance = -20 / +30 μm
Wafer thickness	180	200	220	μm	
Wafer size		150		mm	
Bump pitch	500			μm	
Bump height	72.5	85	97.75	μm	
Bump diameter		110		μm	
UBM diameter	85	90	95	μm	

Table 7 ■ Pin Coordinates for PE42524^(*)

Pin #	Pin Name	Pin Center (μm)	
		X	Y
1	GND	1128.5	-958.5
2	GND	731.5	-646.5
3	V1	253.5	-958.5
4	V2	-253.5	-958.5
5	GND	-1128.5	-958.5
6	GND	-731.5	-646.5
7	RF1	-785.5	-121.5
8	GND	-931.5	363.5
9	GND	-1091.5	913.5
10	GND	-503.5	753.5
11	RFC	0	629
12	GND	503.5	753.5
13	GND	1091.5	913.5
14	GND	931.5	363.5
15	RF2	785.5	-121.5
16	GND	253.5	183.5
17	GND	253.5	-326.5
18	GND	-253.5	183.5
19	GND	-253.5	-326.5

Note: * All pin locations originate from the die center and refer to the center of the pin.

Figure 15 ■ Pin Layout for PE42524⁽¹⁾⁽²⁾



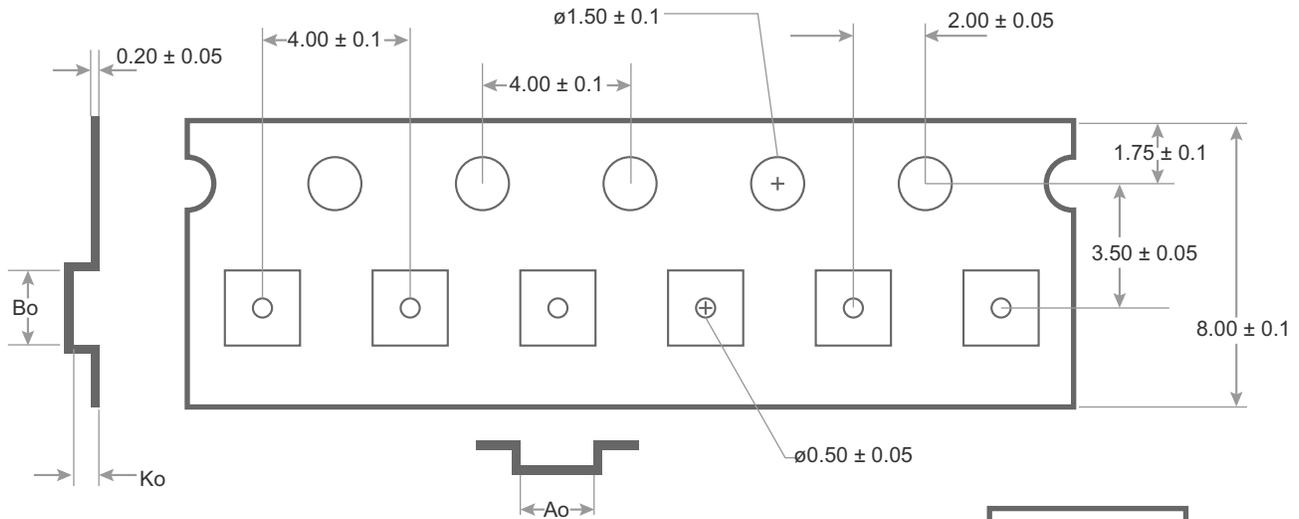
Notes:

- 1) Drawings are not drawn to scale.
- 2) Singulated die size shown, bump side up.

Tape and Reel Specification

This section provides the tape and reel specifications for the PE42524.

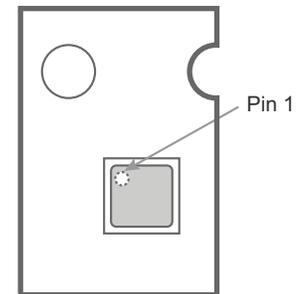
Figure 16 ■ Tape and Reel Specifications for PE42524



Pocket	Nominal	Tolerance
Ao	2.35	± 0.05
Bo	2.66	± 0.05
Ko	0.395	± 0.05

Notes:

Not Drawn to Scale
Dimensions are in millimeters
Maximum cavity angle 5 degrees
Bumped die are oriented active side down



Device Orientation in Tape

Ordering Information

Table 8 lists the available ordering code for the PE42524 as well as shipping method.

Table 8 ■ Order Code for PE42524

Order Code	Description	Packaging	Shipping Method
PE42524B-X	PE42524 SPDT RF switch	Die on tape and reel	500 die / T&R

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. pSemi reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event pSemi decides to change the specifications, pSemi will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Product Brief

This document contains a shortened version of the datasheet. For the full datasheet, contact sales@psemi.com.

Sales Contact

For additional information, contact Sales at sales@psemi.com.

Disclaimers

The information in this document is believed to be reliable. However, pSemi assumes no liability for the use of this information. Use shall be entirely at the user's own risk. No patent rights or licenses to any circuits described in this document are implied or granted to any third party. pSemi's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the pSemi product could create a situation in which personal injury or death might occur. pSemi assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

Patent Statement

pSemi products are protected under one or more of the following U.S. patents: patents.psemi.com

Copyright and Trademark

©2023, pSemi Corporation. All rights reserved. The Peregrine Semiconductor name, Peregrine Semiconductor logo and UltraCMOS are registered trademarks and the pSemi name, pSemi logo, HaRP and DuNE are trademarks of pSemi Corporation in the U.S. and other countries.